DE LA RECHERCHE À L'INDUSTRIE



# leti



**Annual Research Report 2014** 

Silicon Technologies and Components





**Leti** is an institute of **CEA**, a French research-and-technology organization with activities in energy, IT, healthcare, defence and security.

By creating innovation and transferring it to industry, Leti is the bridge between basic research and production of micro- and nanotechnologies that improve the lives of people around the world.

Backed by its portfolio of 2,200 patents, Leti partners with large industrials, SMEs and startups to tailor advanced solutions that strengthen their competitive positions. It has launched more than 50 startups. Its 8,000m² of new-generation cleanroom space feature 200mm and 300mm wafer processing of micro and nano solutions for applications ranging from space to smart devices. Leti's staff of more than 1,700 includes 200 assignees from partner companies. Leti is based in Grenoble, France, and has offices in Silicon Valley, Calif., and Tokyo.

Visit www.leti.fr for more information

Within CEA-Leti, Silicon Technologies and Components research activities are shared between two divisions gathering together around 600 researchers.

**The Silicon Technologies Division** operates 24 hours a day, 7 days a week, all year round, 7,500m<sup>2</sup> of state-of-the-art cleanroom space divided into three different technological platforms.

**The Silicon Components Division** carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend "Moore's Law" for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, power devices, imaging technology, and new types of memory, to enable new applications.







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#### **Dear Reader**

We are proud to release our fifth annual Silicon Components and Technologies Annual Scientific Research Report, for the year 2014. This booklet contains 56 one-page research summaries covering advances in the focus areas of our Silicon Divisions, highlighting new results which have achieved at least two publications during the year.

In 2014, the Silicon Divisions produced 413 publications, including 85 in peer-reviewed journals, achieving Impact Factors as high as 21. We published 435 grade-A items, which include peer-reviewed presentations at international technical conferences sponsored by scientific organizations, peer-reviewed journal papers, and internationally awarded patents.

I am particularly proud to highlight our 17 oral presentations at the 2014 International Electron Device Meeting (IEDM), held in San Francisco last December, which included four invited talks [1-4]. This is an exceptional accomplishment for the Silicon Divisions, placing CEA-Leti in the top tier of institutions worldwide at the major flagship conference on electron device research. It is even more exceptional because we demonstrated the maturity reached by FDSOI and its ability to foster future 2D and 3D applications, as well as the co-integration and achievements of More Moore and More than Moore devices.

More specifically, at nodes below 10nm, active device architecture will be strongly dependent on the control of channel electrostatics and geometric variability. In this dimensional range, we need to envision a reduction of intrinsic variability towards zero. To this end, 1D nanowires and atom-thick 2D materials are good candidates for co-integration in an augmented 3D Si-based Diversified CMOS platform [1].

Power consumption at the system level can be reduced to zero thanks to opportunities in materials engineering, device architecture, heterogeneous combinations of More Moore and More than Moore devices, and packaging [1,2]. Energy supply and storage can be implemented by incorporating adapted harvesters and thin-film batteries [1].

The heterogeneous co-integration of Nano-Electro-Mechanical Systems (NEMS) and CMOS enables high-resolution gas sensing with better figures of merit (signal-to-noise ratio, speed, power consumption) compared to standalone solutions [2]. Nanowire technology can be leveraged to achieve NEMS cantilever multi-gas sensor gauges.

Memory hierarchy revision gives new opportunities to low-voltage switching embedded non-volatile resistive memories (RERAMs) [3]; these can be integrated with logic, for applications beyond data storage. Conductive Bridge RAMs and Ox-RAMs are good candidates for the applications [3]. They will enable drastic new architecture-based improvements in power consumption, latency and design through circuits with reconfigurable, programmable or neuromorphic architectures [3].

Communication with the outside world will be essential to future systems' autonomy and connectivity. SOI substrates, with high resistivity and trap options, have brought major advantages for optimization of front-end component integration, thanks to the reduction of parasitic losses in both passive and active devices, as well as superior isolation compared to bulk [4].



All these subjects have been among our top priorities since I defined the scientific direction of the Silicon Divisions. I am proud to see CEA-Leti keeping its leadership position with a clear vision of the advanced SOI roadmap for 2D&3D co-integration of More Moore and More than Moore devices.

In 2014, Silicon Components and Technologies Divisions members received 76 awards and distinctions – resounding recognition from their peers serving on high-level committees, at societies and with the technical programming groups of international conferences. In addition, our assignees and their co-workers received 12 awards and recognitions of personal distinction from their peers, at conferences and by selection committees. Our researchers won eight awards at international conferences. These honors were earned through strong collaborative teamwork and commitment, and our senior staff members were distinguished four times by their peers.

During the past nine years, I have been very happy to establish and oversee the scientific direction of the Silicon Components and Technologies Divisions (which included 1013 members at the end of 2014). We have created the necessary tools to manage scientific objectives, long-term roadmaps, the selection and review of thesis topics (some 35 new subjects per year and follow up of more than 140 PhD students), internships (about 50 new subjects each year) and post-doctoral research (15-20 new subjects annually).

The value of this activity can be measured through scientific performance, such as publications in highlighted conferences and peer-reviewed journals (a total of more than 400 per year on average), achievement of more than one grade-A publication per potential publishing researcher, exceptional funding such as ERC Grants (three awarded to the Silicon Divisions in the past five years), and international awards and recognitions from our peers. Because patents are vital to our partners' future success, our publication activity is complemented by intellectual property activity – 2014 saw 132 patents filed, 123 with international award.

The special position held by our Silicon Divisions requires committed support of our development activity and maintainance of top-quality research, while retaining strong connections to fundamental academic investigation. This commitment is illustrated by our fostering of long-term efforts through internal CEA Flagship programs, such as ZeroPOVA and A3DN. This continues a multi-decade Silicon Divisions tradition of offering state-of-the-art technology platforms to the scientific community, with the support of CEA.

Our visibility and international recognition are made possible by our international collaborations with major teams at Tokyo Institute of Technology, Caltech, Stanford University, the University of California, Berkeley; École Polytechnique Fédérale de Lausanne, and Albany-Nanotech; and by our participation in major international conferences through technical program committees, boards of governors, and evaluation committees. Underlying all these efforts is the cooperation of all our researchers and management, as well as the Silicon Division scientific committee that I had the pleasure and honor to establish and lead.

I wish great luck to my successors and greetings to the entire staff of the Silicon Components and Technologies Divisions. I also wish to extend my appreciation to the 10 chapter editors and authors of the 2014 Scientific Report, who spared no effort to make it a valuable reference document.

I advise my dear colleagues to keep in mind the popular saying: "Before the baobab grew up (several decameters span), the seed was there (several centimeters in size)." The Silicon Technologies and Components Divisions have demonstrated this principle in the past and have strong assets to continue demonstrating it into the future.

Grenoble, April 10, 2015,

Simon Deleonibus, Chief Scientist, CEA Research Director, IEEE Fellow

#### Invited papers at IEDM 2014, San Francisco, USA, Dec 15-17, 2014

[1] S. Deleonibus *et al.*, "Future Challenges and Opportunities for Heterogeneous Process Technology. Towards the Thin Films, Zero Intrinsic Variability Devices, Zero Power Era".

[2] J. Arcamone et al., "Nanosystems Monolithically Integrated with CMOS: Emerging Applications and Technologies".

[3] E. Vianello *et al.*, "Resistive Memories for Ultra-Low-Power Embedded Computing Design".

[4] C. Raynaud et al., "Technology Pathfinders for Low Cost and Highly Integrated RF Front End Modules".





#### **Dear Reader**

The global semiconductor industry achieved record sales of \$336 billion in 2014 - but will that trend continue in years to come? Today there are many significant uncertainties.

Our technological roadmaps are grappling with the potential end of Moore's law, the complexity of FinFET, FDSOI adoption, delays on 450mm and extreme UV lithography, and other challenges. Our collaborative models and alliances are faced with the multiplication of mergers, changing relationships between fabless companies and foundries, and the growth of the Chinese ecosystem. And future market development hinges on a wide range of factors, including the Internet of Things, Big Data, High Performance Computing and servers, and e-health.

In this evolving context, our division has reaffirmed its world-leading position in nanoelectronics research and, once again in 2014, delivered cutting-edge technology solutions to its industrial partners.

In particular, the work done by CEA-Leti on FDSOI has enabled STMicroelectronics to convince Samsung and GlobalFoundries of the industrial importance of this technology, which offers an excellent alternative to FinFET thanks to a positive trade-off between performance (speed, power consumption, etc.) and manufacturing cost. Meanwhile, we obtained important results on power electronics, which allowed us to establish new partnerships to advance our GaN-on-silicon technology and help create a global technology ecosystem. Finally, we successfully continued the globalization strategy of our MEMS activities. Today, Leti is widely seen as one of the world-leading laboratories in our field, and this greater visibility brings us new clients.

Without being exhaustive, I would like to highlight some major breakthroughs from 2014.

#### **CMOS**

- We demonstrated the dynamic performance of 14nm FDSOI devices, demonstrating their competitiveness with 14nm FinFET. Also last year, 28nm FDSOI achieved production maturity at Samsung Electronics Corp., stemming from a process codeveloped by Leti and STMicroelectronics.
- We proved the implementation of our innovative CoolCube<sup>™</sup> concept on 300mm wafers in a production environment. CoolCube<sup>™</sup> aims at sequential fabrication of vertically stacked transistors and offers true benefits of going to the vertical dimension, because the stacked layers can be connected at the transistor scale. This new technology has attracted interest from Qualcomm and other companies, including IBM, ST and Altera.
- We recorded notable results on memories, including the first functional demonstrator of 12Mbit PCM memory incorporating Leti's phase-change material, and demonstration of more than 100 million cycles on a OxRAM memory built using STMicroelectronics' 28nm CMOS technology.



■ Finally, we realized the 3D assembly of two 65nm logic chips connected by an asynchronous network on chip (NoC) – a world first! This is the result of excellent collaboration, internally between our design and silicon divisions, and externally with partners ST and Mentor Graphics.

### **Power Electronics and Energy**

- Investments made in power electronics have started to bring positive results: realization of GaN power transistors on Si substrates with 30A current capability and 600V breakdown voltage, and strong patent activity (12 patents registered in 2014 on our innovative Normally-Off architectures).
- The start-up Exagan, created in April 2014, fulfills the desire to establish in France a real industrial ecosystem around GaN on silicon. The startup has a fab-lite model, keeping the technological capability to fabricate GaN wafers using GaN epitaxy on 200mm silicon, but outsourcing power component production to a foundry.
- In collaboration with Soitec and the Fraunhofer ISE, we achieved a new world record in the field of concentrated photovoltaics (CPV) with a conversion efficiency of 46.5% measured by the Fraunhofer (or 46% measured by the AIST).
- In the field of thin-film batteries, we supported STMicroelectronics' ramp-up of EnFilm™ technology.

#### **Microsystems**

- We demonstrated a "combo" sensor made of three accelerometers, three gyroscopes, and three magnetometers co-integrated on the same die.
- First images were obtained with an ultrasound probe made by VERMON that integrated our cMUT sensors.
- We established a new state-of-the-art benchmark on BAW filters with Lithium Niobate resonators, which exhibit an exceptional electromechanical coupling coefficient (kt² = 59%). This opens the door to wide-bandwidth filters and new concepts of tunable acoustic filters.
- We supplied our spinoff start-up WAVELENS with a functional MEMS autofocus capability, and they obtained their first prototyping request from big players in the smartphone industry.
- We developed a new concept of 60GHz silicon-integrated antennas based on surface high-impedance (SHI) reflectors and realized through 3D integration. It combined high integration and performance.

All these results were obtained due to the sustained efforts of our team members, and I would like to sincerely thank all of them. Their excellent scientific work was recognized again in several papers at major conferences, including IEDM, VLSI, and Transducers. This report provides an overview of their many achievements.

Grenoble, April 13, 2015 Jean-René Lèquepeys, Head of Silicon Components Division





#### **Dear Reader**

The mission of our division is to provide our internal and external customers with the best innovative engineering solutions, so they can perform world-leading research on next-generation technology nodes. To achieve this, we need to provide the most advanced research facilities in the industry. Therefore, we are continuously investing in new buildings and new process tools.

In 2014, we realized 28.5M€ investment in new manufacturing equipment. This figure includes 4.3M€ dedicated to upgrading our installed base and streamlining our equipment portfolio. Tools put into production last year included latest-generation 300mm as well as online metrology and offline characterization equipment.

Our cleanroom upgrades are continuing; late last year we added 500m<sup>2</sup> to our 300mm line. Moreover, we have begun building a new cleanroom dedicated to photonic-on-silicon processes, with a completion date in 2017.

This internal investment is complemented by a strong policy of collaboration with tool manufacturers. The idea is to build win-win partnerships. CEA-Leti takes advantage of innovative tools or materials to develop next-generation technologies. In return, our partners gain insight into the requirements needed for future process nodes, enabling them to execute solutions well ahead of global semiconductor industry roadmaps. This resulted in the following achievements:

- We renewed three common labs: one with ASELTA Nanographics to jointly develop e-beam proximity effect correction solutions for both mask writing and maskless lithography (ML2) applications, another with Arkema to address development and industrialization of lithography based on nanostructured polymers, and a third with FEI to use holography and nanobeam diffraction techniques to characterize advanced semiconductor materials for the 22nm technology node and beyond.
- We strengthened and extended strategic partnerships with Applied Materials on the CoolCube<sup>TM</sup> transistor stacking concept, new-generation memories and advanced CMOS; with Lam Research on III-V materials etching; and with EVG to optimize temporary and permanent bonding technologies related to 3D TSV integration.

The year also was rich in scientific results for our division with a record number of more than 200 scientific papers produced and more than 40 patents filed. The international recognition we received (six distinctions and awards obtained in 2014) proves the excellence of our teams and their accumulated skills and expertise.



Our team is focusing on key challenges around advanced CMOS, 3D, photonics and advanced memories. We are also addressing key 200mm challenges around MEMS, power electronics, RF, magnetic materials, and other fields. Examples of our achievements include:

- A team comprised of CEA-Leti, Debiotech SA, the Swedish Royal Institute of Technology (KTH) and Mecaplast SA won a silver medal in the 2014 Medical Design Excellence Awards for a MEMS-based micro-needle that allows precise, pain-free injection of up to 0.5ml of vaccines and medications in a few seconds.
- Through common work with Clinatec Institute, we realized a new platform based on porous silicon, dedicated to versatile and efficient detection of biomarkers.
- We transferred know-how to Toyota on the characterization of dopants in SiC devices.
- We developed a new 300mm CMP process for 3D integration of imagers.
- We developed a new directed self-assembly (DSA) process. It can, independent of guide density, properly direct alignment, thus relaxing the resolution requirements of the lithography process.
- We advanced an innovative TEM characterization technique with a sample holder that allows in-situ and in-operando use at atomic scale on semiconductor devices.
- We incubated a start-up focused on ultra-sensitive and ultra-fast Raman spectroscopy, to overcome the limitations of existing analysis techniques (speed, cost, bulky equipment, etc.).

This scientific annual report includes additional details about all these key achievements, which were made possible by the work of our researchers and technicians. I would like to take this opportunity to thank all of them for their constant commitment.

Grenoble, April 14, 2015
Fabrice Geiger, Head of Silicon Technologies Division









607 Permanent Staff 222 Industrial Residents 147 PhD Students 37 Post-Docs

200 & 300mm Platforms for CMOS and MEMS
7,500 m<sup>2</sup> Clean Rooms
500 Process Tools
Continuous Operation





132 Patents Filed in 2014 413 Scientific Papers Produced in 2014

16 Common Laboratories 1 Startup Company Created in 2014







**The silicon divisions** operate 7,500m2 of state-of-the-art cleanroom space divided into three platforms, gathering 500 process tools and a combined staff of more than 450; they run industry-like operations, 24 hours a day, 7 days a week, all year round.

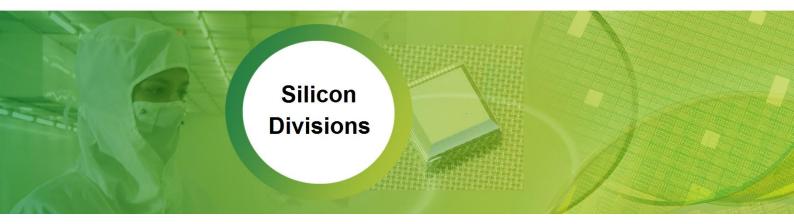
- The Nanotech200&300 platform provides 200mm and 300mm CMOS wafer processing, which can be applied to both semiconductor and microsystem devices.
- The MEMS200 platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS).

Both platforms are focused on the More than Moore initiative to develop new semiconductor capabilities. An innovative cleanroom shuttle system now links the two platforms to add process flexibility and faster processing.

- The third platform 3D Integration aims to integrate various microelectronics objects together in order to juxtapose complementary functions (such as sensing, storing, processing, actuation, communication and energy scavenging) hence providing advanced system solutions in 3 dimensions. This line is open to our customers for prototyping through the Open3D service.
- All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers 8 domains of competencies, including electron microscopy, X-ray diffraction, Ion Beam analysis, optics, magnetic resonance, scanning probe, surface analysis and sample preparation.







#### **Silicon Technologies division** is organized according six departments.

- Three Process Departments: their missions are to realize generic process steps for all projects and to develop innovative processes to provide state-of-the-art solutions to internal and external customers. Those departments are focused on patterning, deposition, and surface treatments. Their research activities in collaboration with key universities allow LETI's advanced position in the future.
- A Characterization Department: its mission is to perform off-line observations to characterize process steps, materials or components. This department also has a research activity to maintain its level of excellence.
- Two Support Departments: one is in charge of the planning, the interface with internal divisions or external customers as well as methods, training and clean-concepts. The other is responsible for facilities operations and engineering.

**Silicon Components Division** is organized around three departments with clear objectives and market focus.

- MOS Department mission is to simulate, model, develop, demonstrate and test new generations of circuits and modules for sub-20nm CMOS, digital and memory.
- MEMS Department mission is to design and develop innovative microsystem components (sensors, actuators and RF) and associated toolbox (packaging, heterogeneous integration, reliability).
- Power and Energy Department is to develop and demonstrate technology modules and components for power and energy (photovoltaic, power electronics, integrated storage).





#### **Publications**

In 2014: 413 publications produced

Ratio "A grade published items/ Publishing researchers" = 1.00 (including grade A conferences, journals and international extended patents)

#### **Distinctions and Awards**

12 distinctions and awards obtained in 2014

- Best Student/Young Scientist Award MRS Spring Meeting 2014 (San Francisco), Manuela Aoukar et al.
- Bronze Medal, 2014 Junior Scientist and Industry Annual Meeting (Grenoble), Larissa Djomeni et al.
- Outstanding Student Paper Award, 2014 ECS Fall Meeting (Cancun), Paul Gondcharton et al.
- Outstanding Student Paper Award, 2014 ECS Fall Meeting (Cancun), Damien Massy et al.
- Best Paper Award, EPTC2014 (Singapore), Sebastien Mermoz et al.
- Young Scientist Award 2014, EMRS (Lille), Viktoria Gorbenko et al.
- 1<sup>st</sup> Prize Art & Sciences Contest, 2014 Int. Conf. On Electron Microscopy (Krakow), Cyril Guedj et al.
- Best Student Paper Award, IMAPS 2014 (San Diego), David Laloum et al.
- Simon Deleonibus, Visiting Professor at Tokyo Institute of Technology, Japan.
- Simon Deleonibus, Chair IEEE Electron Device Society, Region 8 (Europe-Russia, Africa, Middle East).
- Simon Deleonibus, IEEE Transactions on Electron Device, 6 Years Editor Award.
- Simon Deleonibus, IEEE Electron Device Society Board of Governors, 6 Years Elected Member Award.

76 added Awards among which 2005 Grand Prix Académie des Technologies, 2008 IEEE Cledo Brunetti Award, 2011 French-German Prize for Economy, 2011 Silver Medal ST Microelectronics, 2012 SEE Grand Prix du Général Ferrié, 3 ERC Grants, 48 Best Papers Awards.

#### **Expertise and Recognitions**

97 CEA experts: 4 Research Director, 7 International Experts

25 Researchers with habilitation qualification "HDR" (to independently supervise doctoral candidates).

1 IEEE Fellow, 3 IEEE Seniors

#### **Scientific Committees**

3 Journal Editors: IEEE TED, European Physical Journal-Applied Physics, Science China-Information Sciences.

7 researchers involved in ITRS (International Technology Roadmap for Semiconductors)

40 members of Technical Programs and Steering Committees in major conferences:

IEDM, VLSI Technology Symposium, IRPS, ESSDERC, SSDM, ECTC, ECS...

Awards committees: IEEE Cledo Brunetti Award, IEEE Paul Rappaport Award, SEE & IEEE Brillouin-Glavieux Award, European Research Council Panel

Boards of Governors: IEEE ED Society, Nanosciences Foundation Board, IEEE CPMT, SFV IEEE ED Society Region 8 Vice-Chair

#### **International Collaborations**

Collaborations with more than 50 universities and institutes worldwide

Tokyo Institute of Technology, CALTECH, University of Stanford, University of Berkeley, University of Cambridge, University of Tokyo, EPFL, Albany-NT, ...



### PhD Degrees Awarded in 2014



**Bilel SAIDI**University of Toulouse

### Metal Gate Work Function Modulation Mechanisms for 20-14nm CMOS Low Thermal Budget Integration

Since the 45nm CMOS technological node, the microelectronics industry replaced the historical SiO<sub>2</sub>/polysilicon gate stack by the high permittivity oxide (HK)/metal gate (MG) couple. If this choice solved the problem of undesired leakage currents, other difficulties appeared due to the uncontrolled interdiffusion and reactivities of the new gate materials. This is the consequence of the high thermal budget required for the CMOS integrated in the gate first fabrication process. To minimize these difficulties, one option consisted in implementing a new integration scheme with a lower thermal budget like the so-called "gate last" process. In the frame of this approach, gate materials are needed today for the sub-20nm complementary MOS (CMOS) technological nodes in particular for low-power mobile applications (smart phone, ebook). To fit the International Technology Roadmap for Semiconductors requirements, gate materials deposited on HfO2 (the chosen high permittivity oxide that replaced SiO<sub>2</sub> in microelectronics since 2007) with sub-nm equivalent oxide thickness (EOT) control and effective work function (EWF) relevant for nMOS and pMOS co-integration (CMOS) are required. TiN was already a well-known pMOS compatible metal electrode for HfO2. Finding CMOS compatible gate materials with an n-type character was more challenging. For this, we investigated layers of reactive materials deposited on TiN. Single metals like Ti and Al and the binary metallic system TiAl were considered. Then, the case of the ternary TiAlN metal alloy directly deposited on HfO<sub>2</sub> with different N content was examined. We particularly focused our effort on understanding the origins of the electrical parameters (EWF and EOT) variations measured after a low thermal budget process (T≤400°C). A systematic investigation of the elemental distributions across the stack and of the chemical environments was performed by physico-chemical methods (spatially resolved STEM EDX/EELS, TOF-SIMS and back-side XPS) in addition to thermodynamic considerations. By this way, we determined the particular behavior of N and O with respect to Ti, Al and the binary TiAl and their impact on the electrical parameters. The chemical species interdiffusion, in particular their distribution at HK/MG interface, is correlated to the electrodes EWF modulation. Besides, the EOT variation is related to the remote oxygen scavenging from the SiO<sub>2</sub> interfacial layer that is always present between the Si substrate and the HK. This phenomenon induced by the AI, Ti or TiAI metals has been understood on the basis of an advanced thermodynamic study of these materials behavior with respect to oxygen including their free energy of oxide formation and oxygen solubility. Results obtained were helpful to understand the more complex case of the ternary TiAIN metal alloy directly deposited on HfO<sub>2</sub>. By simply varying the N content, this electrode defines the best compromise for a variable EWF compatible for both nMOS and pMOS with a sub-nm EOT. The thermal stability of these electrodes is shown to be limited to temperatures going from 500°C to 700°C depending on the stack considered (TiN/AI, TiN/TiAl or TiAlN). Innovate was another aspect of our work. Therefore, we proposed alternative gate materials. Ta and Ni were studied with different configurations and alloyed with different metals on HfO2 (TaN/Ta, Ta/Ni, Ni/Ti). Here again, the thermodynamic behavior with respect to oxygen and nitrogen and the thermal stability of these innovative electrodes is evaluated to understand their different performances compared to HfO<sub>2</sub>/TiN(Al)-based gate stacks. In particular, Ni/Ti alloying is shown to be very promising for a CMOS co-integration at low thermal budget (T≤600°C) in gate last approach.



Assawer SOUSSOU
University of Grenoble

### Modeling and Characterization of Electrical Effects of Ge Integration in Metal/High-k/SiGe MOS Structures

Maintaining good threshold voltage (VT) centering is a paramount challenge for CMOS technology. The SiGe introduction in bulk and FDSOI pFETs requires VT control for such devices. To this end, we have to extract accurately electrical parameters and to understand Ge integration effects in SiGe based pFETs. In this thesis, first, we have proposed extraction methods to determine VT, at band voltage (VFB) and equivalent oxide thickness (EOT) parameters in bulk and FDSOI transistors. The extraction methods have been validated via Poisson-Schrodinger (PS) simulations and successfully applied to measurements. Second, we have highlighted and explained electric effects of Ge on pMOS gate stack parameters. Electrical characterizations compared with PS simulations have evidenced an additional effective work function increase, induced by Ge, related to interfacial dipoles. STEM, EELS and SIMS characterizations have demonstrated that dipoles are located at SiGe/IL interface.





Yohann SOLARO
University of Grenoble

### Conception, Realization and Characterization of Innovative ESD Devices for FDSOI Technologies (28nm and 14nm Nodes)

Electrostatic Discharges (ESD) are a recurrent problematic faced by the microelectronic industry, compromising the reliability of integrated circuits. Moreover, dimensions shrinking of the transistors, caused by the pursuit of performance enhancements of the CMOS circuits make ESD protection design more and more difficult. FDSOI architecture (Fully Depleted Silicon On Insulator) allows a significant improvement of the electrostatic behavior of the MOSFETs transistors for the advanced technologies. It is industrially employed from the 28nm node. However, the implementation of ESD protections in these technologies is still a challenge. While the standard approach relies on SOI substrate hybridization (by etching the BOX (buried oxide)), allowing to fabricate vertical power devices, we focus here on structures where the current flows laterally, in the silicon film. In this work, several solution of the literature are first reviewed. Alternative approaches are proposed for the 28nm and 14nm FDSOI technologies. They use innovative "band modulation" devices (Z2-FET and BBC-T). Their static, quasi-static and transient characteristics are studied, with TCAD simulations and electrical characterizations. Different optimizations are studied, from the technology and the design point of view, allowing improving the low and high current characteristics of these new protection elements. In particular, the influences of parameters such as the geometry, biasing conditions, thicknesses, or doping levels are analyzed in detail.



### Heimanu NIEBOJEWSKI University of Lille

#### Self-Aligned Contacts for the 10nm FDSOI CMOS Technology

For sub-14nm transistor generations, the integration of classical metallic contacts subjected to optical lithography limitations prevents the fulfillment of alignment performance required by design rules (64nm gate pitch for the 10nm node) and industrial yields.

In the frame of this PhD. work, an original transistor architecture featuring self-aligned contacts (SAC) is studied for CMOS FDSOI technologies.

First, a Self-Aligned Contacts (SAC) module has been integrated and validated on a CMOS 14nm FDSOI process flow. The feasibility of SAC integration at a more aggressive gate pitch (10nm node) has also been demonstrated morphologically. The impact of such integration on the transistor and circuit performance, in terms of parasitic capacitances especially, has been evaluated through numerical simulations (TCAD, SPICE) in the case of the 10nm FDSOI technology. Finally, several techniques inducing mechanical stress within the transistor channel have been analyzed in order to improve the device performance. Among those, the use of contacts on source-drain to induce such stress has been particularly investigated.



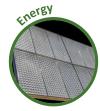
### Thomas CABOUT

### Technological Optimization and Electrical Characterization of Oxide Based Resistive Memories (OxRRAM) for Low Power Applications

Today, non-volatile memory market is dominated by charge storage based technologies. However, this technology reaches his scaling limits and solutions to continue miniaturization meet important technological blocks. Thus, to continue scaling for advanced nodes, new non-volatile solutions are developed. Among them, oxide based resistive memories (OxRRAM) are intensively studied. Based on resistance switching of Metal/Isolator/Metal stack, this technology shows promising performances and scaling perspective but isn't mature and still suffer from a lake of switching mechanism physical understanding.

Results presented in this thesis aim to contribute to the development of OxRRAM technology. In a first part, an analysis of different materials constituting RRAM allow us to compare unipolar and bipolar switching modes and select the bipolar one that benefit from lower programming voltage and better performances. Then identified memory stack TiN\HfO<sub>2</sub>\Ti have been integrated in 1T1R structure in order to evaluate performances and limitation of this structure. Operating of 1T1R structure have been carefully studied and good endurance and retention performances are demonstrated. Finally, in the last part, thermal activation of switching characteristics have been studied in order to provide some understanding of the underling physical mechanisms. Reset operation is found to be triggered by local temperature while retention performances are dependent of Set temperature.

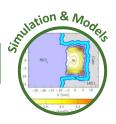




### Raphaël LACHAUME University of Grenoble

### Contribution to the Electrical Characterization and to the Numerical Simulation of the Silicon Heterojunction Solar Cells

By combining the advantages of thin-films and crystalline silicon (c-Si), the silicon heterojunction solar cell technology (HET) achieves a better cost-performance compromise than the technology based only on c-Si. The aim of this thesis is to improve the understanding of the physical mechanisms which govern the performance of these cells by taking advantage of specific characterization and simulation skills taken from microelectronics. Our study focuses on the front-stack of the n type cell composed of thin layers of indium tin oxide (ITO) and hydrogenated amorphous silicon (a-Si:H). We begin with a theoretical and experimental study of the conductivity of a-Si:H layers as a function of temperature, doping concentration and bulk defects density. It is important to properly take into account the dopant/defect equilibrium of these layers but we also show that the work function of the electrodes in contact, such as the ITO, can strongly influence the Fermi level in the nano-films of a-Si:H. Then, we evaluate seven characterization techniques dedicated to the work function extraction in order to identify the most suitable one for studying degenerate semiconductors such as the ITO. We particularly show the interest of using original microelectronics techniques such as capacitance C(V), leakage current I(V) and internal photoemission (IPE) measurements on ITO/bevel oxide/silicon test structures. We clearly demonstrate that the ITO bulk properties can be optimized, yet the interfaces have a major influence on the extracted values of the effective work function (EWF). A good overall consistency has been obtained for C(V), I(V) and IPE measurements on a silicon dioxide bevel (SiO2) ; the extracted values enabled us to explain experimental results concerning the optimization of HET cells. We show that the open circuit voltage (Voc) of these devices is finally barely sensitive to work function, unlike the Fill Factor (FF). This is due to the a-Si:H layer. The more it is doped, defective and thick, the more it is able to screen the electrostatic variations of EWF. Thus, EWF must be sufficiently high to be able to reduce the p a-Si:H layer thickness and, in turn, to gain in short-circuit current (Jsc) without losing either in FF or Voc. Finally, we successfully applied this methodology to other types of transparent conductive oxides (TCO) differing from ITO. The best candidate to replace ITO must not only have a high optical transparency, be a good conductor and have a high EWF, but we must also pay close attention to the possible interface degradations caused by the deposition techniques.



### Benoît SKLENARD University of Grenoble

### Physical Modeling of Junction Processing in FDSOI Devices for 20 nm Node and Below

Complementary metal oxide semiconductor (CMOS) device scaling involves many technological challenges in terms of junction formation, in particular for 3D sequential integration and Fully Depleted Silicon on Insulator (FDSOI) architectures. In this thesis, the physical phenomena involved during the junction formation at a low processing temperature (i.e.  $\leq 600^{\circ}$ C) have been studied. Such a process relies on Solid Phase Epitaxial Regrowth (SPER) of an amorphous region to activate the dopants. A new model based on Kinetic Monte Carlo (KMC) method has been developed in order to simulate SPER at the atomistic scale. This model has been used to understand the regrowth anisotropy and provide an explanation for the formation of defects as well as to get insight into the influence of a non-hydrostatic stress and the presence of electrically active dopants on the regrowth kinetics.



### **Daniele SETTE**University of Grenoble

### Functional Printing: From the Study of Printed Layers to the Prototyping of Flexible Devices

In the last decade, functional printing has gained a large interest for the manufacturing of electronic components. It stands aside to silicon technologies and specifically targets markets of large area devices (screens, photovoltaics) and flexible electronics (RFID antennas, sensors, smart textiles). In this work, inkjet printed silver layers are characterized depending on the printing conditions and the required post-printing annealing. The evolution of their microstructure, electrical and mechanical properties is investigated as a function of the annealing temperature. The correlation of the measurements with theoretical models supports the experimental methods that were developed. The knowledge of the printed silver layers assets and the optimization of the printing process lead to the design, fabrication and characterization of flexible electronics devices: a 17GHz band-pass filter

the design, fabrication and characterization of flexible electronics devices: a 17GHz band-pass filter printed on polyimide, a flexible vacuum micro-sensor working on the Pirani principle, and a 250µm thick membrane switch for keyboards. Finally, all-printed RF capacitors were realized by stacking Barium Strontium Titanate (dielectric) and silver printed layers. These prototypes exhibit performances near the state-of-the-art and suggest new opportunities for printing technologies. This thesis offers a thorough study of inkjet printed silver layers and assess their potential for the manufacturing of flexible devices.





### Julie ABERGEL University of Grenoble

#### **High-Strain Piezoelectric Materials for MEMS Actuation**

Piezoelectric actuators exhibit low response times and high deflection/actuation voltage ratios. This PhD thesis aims at optimizing their strain values by increasing the applied field and the piezoelectric coefficients. To target low voltage issues, Aluminum Nitride (AIN) ultrathin layers were deposited and characterized. e31,eff coefficient was found to be constant between 800 and 50nm, at a value as high as -0.8C/m<sup>2</sup>. Piezoelectric behavior was also shown for 12nm-thick AIN layers, by three different ways. Still in order to apply high electric fields, a study was carried out to improve Lead Zirconate Titanate (PZT) breakdown field, by inserting lanthanum atoms. Breakdown field was improved by approximately 35%, with no decrease of permittivity or piezoelectric coefficients. Another optimization approach consists in increasing the material's piezoelectric coefficients. In this view, PZT was characterized around several phase transitions. Near morphotropic phase boundary, piezoelectric effect was found to be enhanced: e31,eff coefficient raises up to -18 C/m<sup>2</sup> at low field conditions and -27C/m² in actuating conditions. Domain wall pining issue was also discussed. Near Curie transition, dielectric properties were found to be enhanced, with a dielectric constant rising up to 2640 at 370C, which is almost twice as high as room temperature value. Furthermore, dielectric loss decreases from 25C to 280C to reach 1.6%. To profit from a critic phase transition, highly Lanthanum doped PZT was deposited. Relaxor behavior was shown and an induced piezoelectric coefficient d31 of -25 pm/V was measured. Materials developed in this PhD thesis can be used to realize microactuators and especially inkjet print-heads.



### Remy DEJAEGER University of Lyon

### Multi-Physic Modelization, Realization and Characterization of a Piezoelectric MEMS Digital Loudspeaker Array

The Digital Loudspeaker Array (DLA) is an electroacoustic transducer which receives as input a digital signal and performs the analog conversion directly into the air. It consists of a plurality of radiating elements arranged in a matrix. These elements will be designated by the term « speaklet » when they are reduced in size. The acoustic radiation of a DLA is indeed very sensitive to the size of the matrix due to differences in path length, which makes it especially suitable for MEMS technology. This thesis presents study of a piezoelectric MEMS DLA. After an introduction that is increasingly focused on the subject, the thesis addresses the multiphysics modeling of the DLA, dimensioning of the speaklets and experimental tests.

Analytical formulas, numerical simulations and finite element models are developed and used to predict the mechanical behavior of the presented speaklets, the pressure radiated by the DLA and the electrical power consumption. The speaklets are then dimensioned from the technological stack (set in advance) in order to maximize the pressure level. Experimental tests involving the use of an anechoic chamber, an optical interferometer, a vibrometer and an impedance-meter validate most of the models. Otherwise, these tests are useful for improving some of them or for showing their limitations. The results have shown the importance of the residual stresses, which cause an initial deformation of the speaklets and modify their Eigen frequencies, thus rendering ineffective the use of large radii. In accordance with the models, the static deflection of the speaklets is nonlinear but their dynamic behavior is linear. This enables characterizations using transfer functions. Theory and sound recordings show that a DLA made of such speaklets can produce in the best case the same pressure as the one generated by the same matrix driven in an analog way. In our case, more distortions were obtained in digital reconstructions because of non-uniform responses of the speaklets, due to different access resistances. However, the presented DLA has other advantages, the most important being the very low power consumption it is theoretically possible to achieve using the adiabatic charge principle. The piezoelectric MEMS DLA thus appears as a promising technology. The optimization of our first prototype using the developed tools should indeed lead to a DLA able to generate a pressure equivalent to the one obtained with analog control, but with a far greater electroacoustic transduction efficiency. Future work should then focus on the design of nonlinear speaklets and on the shaping of the pulse of pressure they generate, in order to increase the total pressure level.





### Fabrice CASSET University of Lille

### Mechanical Properties Characterization of Thin-Film PZT for MEMS Applications using Picosecond Ultrasonics

MEMS components are today an economic reality and are already used in many mass market applications. These devices can use a piezoelectric actuation, in particular based on thin-film PZT due to its high piezoelectric coefficient. To perform predictive design of high performances components based on PZT actuators, mechanical properties of the PZT are required. We used the picosecond ultrasonic technique which probes thin layers with high frequency acoustics waves generated by ultrashort laser pulses. It allows the transposition of the sonar principle at nanometric scale. During this PhD, we studied thin-film PZT using picosecond ultrasonics. We extracted both Young's modulus and Poisson ratio without an approximation of one or the other. We also studied wall domain relaxation using picosecond ultrasonic measurement at various frequencies. Using PZT mechanical properties obtained from picosecond ultrasonics, we extracted the PZT piezoelectric coefficient, from the comparison between PZT-based cantilever measurement and numerical modeling. Finally, we applied these data for the design of haptic plates using thin-film PZT actuators. The good agreement between haptic plate measurements and modelization proves all the benefit of picosecond ultrasonics for MEMS design.



### Paul IVALDI University of Grenoble

#### AIN based Cantilever Resonator for Gravimetric Gas Sensors

With the development of micro and nano technologies in the last three decades, the performances of gas chemo sensors have been improved drastically, paving the way for new applications. Especially, these new devices with provided low fabrication cost, high sensitivity and miniature size are very good candidates for applications where high performances are required and heavy, expensive and slow instruments such as such GC and MS are not viable technically or economically. This is the case, in particular, for on-field detection of warfare agents, monitoring of indoor air pollution and medical diagnosis. The main objective of this PhD thesis is to investigate the piezoelectric transduction at the nano-scale for the development of high-resolution resonant micro-cantilever based gas sensor. To that mean, we have intended to cover the whole prototyping chain from the development of 50nm thick Aluminum Nitride (AIN) piezoelectric films with good piezoelectric properties to the gas sensing proof of principle experiment using cantilevers resonators actuated and detected piezoelectrically by the mean of these 50nm thick AIN films. We also have covered the theoretical analysis for sensing performance optimization of these devices and their read-out and control electronic circuits.



### Julien PHILIPPE University of Grenoble

### Technology of Fabrication and Work's Analysis of a Nanowires Sensor Co-Integrated CMOS for Medical or Environmental Applications

The Micro Electro Mechanical Systems (MEMS) devices are present everywhere in our daily life, since they are the main component of sensors present in many objects: our cars (airbag, pressure sensors) and our smartphones (microphones, accelerometers) for example. Their sub-µm downscaling has allowed the emergence of a new kind of devices called NEMS (for Nano Electro Mechanical Systems) and the possible use of these systems in specific applications in which a high level of sensitivity and resolution is necessary, such as gas sensing, mass spectrometry and molecules recognition using traditionally bulky machines. This thesis proposes a new way to fabricate mass detectors by implementing both NEMS devices and electronic circuit on the same chip in order to get a compact and high performance sensor for such application.





### Monica Larissa DJOMENI WELEGUELA University of Strasbourg

### Study of Through Silicon Via Integration Realized Through MOCVD for 3D Stacking of Microelectronic Components

For the past years, Moore's law has pointed mainstream microelectronics, driving integrated circuits down to 22 nm and below. Yet, performance, dimension and cost issues make it difficult to follow the trend. Integrating analog functions into CMOS-based technologies enables cost-optimized systems solutions. These diversified tendencies are known as "More than Moore". One of the key technologies of this trend is the TSV, which maintains the contact between two components.

The increasing aspect ratio of via made it critical to obtain a continuous, conformal coverage of the copper diffusion barrier layer using iPVD.

In the first part of this thesis, a promising deposition technique by MOCVD has been developed at low temperature to fulfill various integration schemes including via last and via middle processes.

Characterizations of the behavior of these materials in the TSV then became a great challenge in order to handle the integration protocol. Working at theses scales makes standard methods limited to evaluate the intrinsic properties inside the TSV. In the second part, the implementations of advanced characterization into these structures were carried out.



### Papa Momar SOUARE University of Saint-Etienne

### Thermal Effects in 3D Stacks of Electronic Chip: Numerical and Experimental Studies

Today we are witnessing an evolution of mobile electronic systems to more advanced features. The complexity of mobile electronic systems requires an increase in computing power, which can be achieved either by the use of more aggressive CMOS technology ("Moore's law"), or by a technique called 3D integration ("More than Moore"). Three dimensional (3D) stack of electronic chips generates an increase of the power density dissipated per unit area. This power, essentially resulting from Joule effect in transistors and interconnections, contributes to increase the overall temperature of the stack. The global objective of this thesis is to study the heat transfer in a 3D stack of chips during operation. We will focus on understanding the geometric and materials effects of the stack and the impact of the placement of 3D interconnects (TSV, Bumps ...) on these heat exchanges. The study relies on both numerical simulations and experimental measurements on 3D stacks that validate the numerical model. These numerical and experimental studies can also be used to establish thermal design rules, especially for 3D interconnects placement and design. The establishment of such a thermal model is based on finite element simulations of an industrial 3D process in CMOS 65nm node. This allows an unprecedented accuracy in our thermal model. Indeed, previous simulations used compact models less accurate than finite elements - and a generic method that does not reflect all of the properties of materials and in particular interfaces. In the experimental part, accurate thermal mapping of the 3D stack are obtained using a large number of sensors embedded in the silicon, and under different conditions of 3D chip process. This provides a numerical model validated and calibrated by experimental measurements.



### Julien BERTHEAU University of Grenoble

### Study and Characterization of Intermetallics Interconnections based on Copper Pillars and SnAgCu Alloys for 3D Integration

Technological roadmap of the microelectronic industry is mainly described by Moore's law which aims a constant reduction of transistors size. Three-dimensional integration of active chips appears more and more as an alternative way to Moore's law. According to this strategy, chips are interconnected along the vertical axis thanks to copper pillars and a tin based alloy (SnAgCu). The joining is then performed through eutectic bonding using a SnAgCu solder alloy which is at the origin of intermetallic compounds growing at the copper alloy interface. These intermetallic compounds are sometimes described in literature as weakening factor of the interconnection mechanical reliability. Moreover this interfacial reactivity leads also to the formation of Kirkendall microvoids potentially causing interconnections breakings, mostly noticed during ageing tests.

This report is dedicated to the study and metallurgical characterization of the interconnection system with a size close to that of the actual prototypes which is 25µm. The study is successively focused on SnAgCu alloy microstructure, Cu/SnAgCu and Ni/SnAgCu interfacial reactivity and on the mechanical reliability of interconnection system. These topics are investigated in function of thermal constraints and during different integration steps until chips packaging. The main critical aspect is related to the fact that system dimensions, already small, are planned to be reduced, leading to a more important proportion of the solder alloy consumed by interfacial reaction.





### **Hélène ISSELE**University of Grenoble

### Characterization and Modeling of Mechanical Properties of Thin Films for the Manufacture of Microelectronic Devices - Application to the Field of 3D Integration

The fabrication of microelectronic devices using 3D integration technologies requires a good knowledge of mechanical issues. Indeed, the thin films that are integrated have various thermomechanical properties and are deposited onto a substrate that is thinned in order to carry out the interconnections. The level of stresses and strains in devices has to be strictly controlled during their processing.

The goal of this work is to exploit the characterization techniques available at the CEA-Leti and to couple them with modeling tools to address this issue. This coupling is used to control the mechanical behavior of a complex stack at each step of its fabrication. The experimental techniques that are used are non-destructive. The modeling tools take into account the elastic and thermal properties of each material involved in the stack, and also the intrinsic strains caused by the deposition of each layer. Coupled methodologies have been carried out to evaluate these input data. From a material database, a tool to predict the mechanical behavior of a multilayer stack was developed and validated experimentally. It enables to predict the level of strain and stress of the stack.

Mechanical predictions enable to guide the selection of materials in order to improve the devices integrity and optimize their fabrication. Reliability issues that occur in the long term, due to a significant level of stress and strain can also be anticipated.



### Anthony VILLALON University of Grenoble

### Steep Slope Nano-Transistors for Ultra Low Power Applications

Band to band tunneling field effect transistor (TFET) is a PIN-gated architecture able to reach sub 60mV/dec subthreshold slopes at room temperature, which is an advantage over MOSFET in low power applications. The objective of this thesis is to study and characterize TFETs fabricated in CEA-Leti using MOSFET SOI technology. The first generation of devices is realized on planar FDSOI technology, and studies the impact of source/channel heterojunction, channel thickness and annealing temperature on device performances. The second generation is planar SiGe nanowire architecture, with research focusing on the impact of the wire geometry. Through measurements we were able to prove the band to band tunneling injection, while the reported performances were compared with literature and with MOSFET. Furthermore, advanced characterizations led to a better understanding of the output characteristics. Through low temperature measurements we confirmed existence of defects close to the junctions (which cause slope degradation), as well as on which process steps to improve in the future.



### Fabien PIALLAT University of Grenoble

### Plasma Assisted Chemical Deposition (CVD/ALD) and Integration of Ti(Al)N and Ta(Al)N for sub-20 nm Metal Gate

Conformity requirements for the sub-20 nm technological nodes metal are beyond the possibilities of the currently used PVD deposition technique. CVD techniques, more specifically MOCVD and ALD, are identified as the best techniques for metal deposition. For metal-gate application, titanium and tantalum carbo-nitrides alloys are considered as the most promising. In this work, a detailed review of MOCVD and ALD deposition mechanisms and plasma influence on the deposited material is carried out. First, process windows for successful tuning of the metal properties are examined. Plasma impact on the metal and the inherent reaction mechanisms are also highlighted with the help of plasma characterization. Then great importance is given to the integration of these metals, by careful study of the interactions taking place at the interfaces. Correlations between physico-chemical properties and electrical behavior of the metal/high-k dielectric stack are introduced thanks to XPS characterization. Finally, aluminum doping of MOCVD TaN is considered for n-mos and p-mos gate characteristics achievement. By comparison of the properties and behaviors of Al doped metals deposited by PVD and MOCVD, diffusion mechanisms are proposed to explain the role of Al in the observed changes.





### **Damien RADISSON** University of Grenoble

#### **Direct Bonding of Patterned Surfaces**

Direct bonding is a process by which two sufficiently flat and clean surfaces can bond to each other without any added adhesive layer. Direct bonding of patterned surfaces is often used for the fabrication of Micro-Electro-Mechanical Systems (MEMS), where a silicon wafer with cavities is bonded to a plain wafer. The fabrication of these devices is expensive and it would be useful to have quidelines when designing knew devices to know in advance if direct bonding will be possible.

A 2D simulation model of the direct bonding of two substrates is developed and used to study the influence of the cavities on the bonding wave velocity. The prediction of the simulation run with Comsol® are in good coherence with the experimental measures and a 2D law of the bonding velocity is obtained. The bonding of perfectly flat wafers with cavities should always be possible. Limitations to the bonding of real wafers are due to the elastic energy cost of deforming the non-perfectly flat wafers. This limit is reached easily when the bonding wave must cross a trench, so a design with a small bonding guide to help cross the cavity will work best. The width of this wave guide should be chosen by considering the bow of the wafer. Indeed the second important design rule is to keep a bonding area big enough to have more adhesion energy than the elastic energy cost due to non-flat wafers deformation. The adhesion energy is an important parameter of the direct bonding, as it is the energy that drives the adhesion. This adhesion energy is different from the more widely known bonding energy which is the energy needed to separate two previously bonded wafers. In this work a simple method to measure the adhesion is proposed. Long time measurement of the evolution of the adhesion energy lead us to propose a mechanism for its evolution linked to the formation of capillary bridges between rough surfaces.



### Caroline RAUER University of Grenoble

### Silicon and Silicon Dioxide Direct Bonding : Understanding of the Involved Mechanisms

Direct wafer bonding refers to a process by which two mirror-polished wafers are put into contact and held together at room temperature by adhesive force, without any additional material. This technology feasible at an industrial scale generates wide interest for the realization of stacked structures for microelectronics or microtechnologies. In this context, a precise understanding of bonding mechanisms is necessary. Consequently, the aim of this work is to study the bonding mechanisms for hydrophobic silicon reconstructed surfaces and hydrophilic deposited silicon oxides surfaces.

In this study, bonding of hydrophobic silicon reconstructed surfaces and bonding of hydrophilic deposited silicon oxides prepared either by plasma activation or chemical-mechanical polishing were analyzed, as a function of post-bonding annealing temperature. For this, several characterization techniques have been used: bonding energy measurement, acoustic microscopy in order to observe defectivity, infrared spectroscopy and X-Ray reflectivity. Thus the bonding interface closure has been analyzed from a chemical and mechanical point of view and bonding mechanisms have been proposed for the studied bonded structures. Finally the study of deposited silicon oxide bonding prepared either by plasma activation or by chemical-mechanical polishing has led to some recommendations for efficient and high quality deposited silicon oxides bonding.





FDSOI: Advanced Modules and Design

Reliability and Variability Methods for Nano Transistors & Basic Circuit Elements

CoolCube<sup>™</sup> Integration

Very Low Temperature Deposition - Etch of SiGe:B Raised Sources and Drains for CoolCube<sup>TM</sup>

Tunnel Transistors (TFET) & Single Electron Transistors (SET) in Nanowire Architecture on SOI

Advanced Nanowire FET Technology



### FDSOI: Advanced Modules and Design

#### Research topics: CMOS, SOI, FDSOI

B. De Salvo, J. Mazurier, O. Weber, O. Thomas

Partnership: IBM, STMicroelectronics, IMEP-LACH, SOITEC, Berkeley Wireless Research Center Sponsorship: Catrene-Dynamic ULP, Catrene-Reaching 22, ENIAC-Places2Be, Eurotalent

Planar FDSOI is an important device architecture for continued CMOS scaling [1-4] and an attractive alternative to more complex FinFET architectures. Its advantages include: excellent short channel electrostatics, un-doped channels, effective back bias for performance boost and leakage lowering; a more conventional, lower cost process.

In [1], we presented a 14nm FDSOI technology designed for high speed and energy efficient applications using strainengineered FDSOI transistors (i.e. dual SOI/strained SiGeOI N/P channels). Compared to the 28nm FDSOI technology, this 14nm FDSOI technology provides 0.55x area scaling and delivers a 30% speed boost at the same power, or a 55% power reduction at the same speed, due to an increase in drive current and low gate-to-drain capacitance. Using forward back bias (FBB) we experimentally demonstrated that the power efficiency of this technology provides an additional 40% dynamic power reduction for ring oscillators working at the same speed. Finally, a full single-port SRAM offering was reported, including an 0.081µm<sup>2</sup> high-density bitcell and two 0.090µm² bitcell flavors used to address high performance and low leakage-low Vmin requirements.

In view of the 10nm node, we reported in [2] FDSOI devices with a 20nm gate length and 5nm spacer, featuring a 1.3 GPa tensile strained Silicon-on-Insulator (sSOI) channel NFET and 35%Ge partially compressive strained SiGe-on-Insulator (SGOI) channel PFET. At Vdd of 0.75V, competitive effective current (Ieff) reaches 550/340 µA/µm for NFET, at Ioff of 100/1 nA/µm, respectively. With a fully strained 30% SGOI channel on thin BOX (20nm) substrate and Vdd of 0.75V, PFET Ieff reaches 495/260 µA/µm, at Ioff of 100/1nA/μm, respectively. Competitive sub-threshold slope and DIBL are reported. With the demonstrated advanced strain techniques and short channel performance, FDSOI devices can be extended for both high performance and low power applications to the 10nm node. Moreover, a multimodeling (based on mechanical simulations, Noneequilibrium Green's functions simulations, piezoresistance coefficients, mobility analytical modeling, compact modeling) calibrated on state-of-the-art FDSOI devices was also developed [3]. It has been shown that high-mobility gains can be achieved for both NMOS and PMOS (sSOI substrate providing the major NMOS gain (x2); PMOS mobility being improved by a factor 8 both by the Ge fractions increase in channel/RSD and layout optimization (slicing), thanks to the high impact of uniaxial strain). Finally, FDSOI Ring Oscillator simulations showed that a dynamic power gain of 50% could be achieved while maintaining circuit frequency performance, thanks to strain

In [4], we demonstrated the 28nm ultra-thin body and buried oxide (UTBB) FD-SOI high-density (0.120µm²) single p-well (SPW) bitcell architecture for the design of low-power wide voltage range systems enabled by back-bias

adjustment. The results from a 140kb programmable dynamic SRAM characterization test module have provided both information about location and cause of failures as well as power and performance by mimicking system operating conditions over a wide supply voltage range. A 410mV minimum operating voltage and less than 310mV data voltage with less than 100fA/bitcell were retention measured. Improved bitcell read access time and writeability through back-bias were demonstrated with less than 5% of stand-by power overhead.

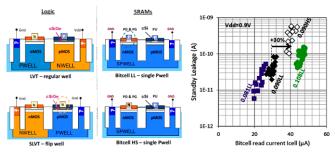


Figure 1: (left) Schematics highlighting logic & SRAM devices construction for multi VT and back bias optimization. (right) Icell vs ISB at Vdd=0.9V for 14FDSOI single port SRAM bitcells (after [1]).

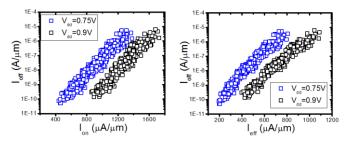


Figure 2: sSOI NFET (left) Ion and (right) Ieff at Vdd of 0.9V and 0.75V (after [21).

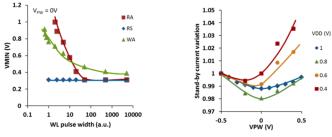


Figure 3: RS, WA, RA VMIN vs WL pulse width (left) and I<sub>OFF</sub> vs VPW.

#### Related Publications:

- [1] O.Weber et al., "14-nm FDSOI Platform Technology for High-Speed and Energy-Efficient Applications", VLSI Techn. Symposium '14.
- [2] Q.Liu et al., "FDSOI CMOS Devices Featuring Dual Strained Channel and Thin BOX Extendable to the 10nm Node", IEDM 2014.
- [3] B. De Salvo et al., "A mobility Enhancement Strategy for sub-14nm Power-Efficient FDSOI Technologies", *IEDM* 2014. [4] O. Thomas et al., " Dynamic Single-P-Well SRAM Bitcell Characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI", IEDM 2014.



# Reliability and Variability Methods for Nano Transistors & Basic Circuit Elements

#### Research topics: FDSOI, Reliability, Dynamic Variability

X. Garros, A. Subirats, J. El Husseini, G. Reimbold

### Partnership: STMicroelectronics, IMEP-LAHC Sponsorship: ENIAC-Places2Be, LabEx-MINOS

Negative Bias Temperature Instability (NBTI) is a key reliability concern which affects the working of digital & analog circuits. To address NBTI issue at circuit level, one standard approach is based on the modeling of the NBTI degradation measured at transistor level stressed under simple AC mode, i.e. an alternate sequence of '1' & '0' bits. Nevertheless, the real stress seen by the device in a circuit is not as regular as in this AC stress. We therefore propose a new fast characterization technique (~1µs range) able to measure the NBTI degradation under arbitrary gate stress patterns (see Fig.1). The stress sequence consists this time in an arbitrary succession of bits '1' or '0' corresponding to 2 gate bias values. This sequence of ~20 bits, called pattern, can be repeated up to 1E12 times. This method allows us demonstrating that the NBTI aging of a device integrated in a circuit mainly depends on the circuit activity and on its working frequency and not on the bits arrangement. An effective modeling was also provided to reproduce accurately the NBTI degradation (solid lines). This model can be integrated in a spice simulator to predict the degradation of a circuit after long working times.

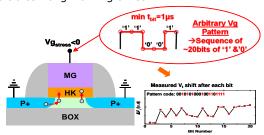


Figure 1: AVGP method to measure NBTI aging under circuit working condition.

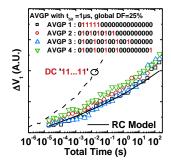


Figure 2: Vt shift induced by NBTI for different AVGPs.

NBTI also induces a temporal variability of threshold voltage Vt in nano-scaled transistors which affects the stability and reliability of a SRAM cell. A new methodology based on the "Supply Read Retention Voltage" (SRRV) metric was

therefore proposed to address this concern in high density SRAM cells made in 28nm FDSOI technology. This technique shown in Fig.3 consists in measuring the read margin of the cell, through a direct measure of the bitline current. The method is equivalent to the butterfly method but it is faster. With this original method it is possible to measure how a BTI stress at strong Vdd impacts the read stability of the cell (see Fig.3 right).

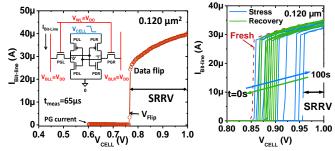


Figure 3: SRRV measurement (left) and its evolution with stress.

Moreover the degradation varies from one cell to another. That is why we are talking about "dynamic variability". This also explains why a statistical analysis must be used to address this issue. Experimental results are shown in Fig.4 and are well modeled by Monte Carlo SPICE simulations. This validates our simulation approach to evaluate the impact of the BTI stress on the PASS/FAIL of a complete SRAM matrix. The key result is that, in standard working conditions of the SRAM cut (VDD=1 V et T<85°C), the impact of BTI on the read stability of the 28nm FDSOI array is very small, even after 10 years working. This methodology based on measurements at the bitcell level is very useful for a complete evaluation of the reliability of large SRAM arrays. In the future, it will be applied to the study of the most advanced technology nodes.

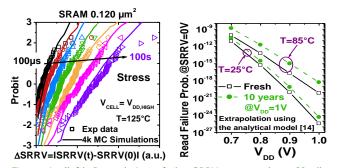


Figure 4: (left) Degradation of the SRRV measured on 60cells at various stress times (right) Read failure probability of 100k SRAM array before & after a 10 years stress at Vdd=1V.

#### Related Publications:

[1] A. Subirats, X. Garros, J. Cluzel, J. El Husseini, F. Cacho, X. Federspiel, V. Huard, M. Rafik, G. Reimbold, G. Ghibaudo, "A new gate pattern measurement technique for evaluating the BTI degradation in circuit conditions", *IEEE Int. Reliability Physics Symp. (IRPS)*, 2014. [2] J. El Husseini, X. Garros, A. Subirats, A. Makosiej, O. Weber, O. Thomas, V. Huard, X. Federspiel G. Reimbold, "Direct measurement of the dynamic variability of 0.120µm2 SRAM cells in 28nm FD-SOI technology", *IEEE Symposium on VLSI Technology*, 2014.

[3] J. El Husseini, X. Garros, J. Cluzel, A. Subirats, A. Makosiej, O. Weber, O. Thomas, V. Huard, X. Federspiel and G. Reimbold, " A complete characterization and modeling of the BTI-induced dynamic variability of SRAM arrays in 28 nm FD-SOI technology", *IEEE Transactions on Electron Devices*, Vol. 61, No. 12, December 2014.



### **CoolCube™ Integration**

#### Research topics: 3D Sequential Integration, Low Thermal Processes

C. Fenouillet-Beranger, P. Batude, B. Mathieu, O. Turkyilmaz

Partnership: STMicroelectronics, IBM, Qualcomm, LASSE Sponsorship: Nano2017

Compared with TSV-based 3D ICs, CoolCube  $^{\text{TM}}$  or sequential 3D ICs presents "true" benefits of going to the vertical dimension as the stacked layers can be connected at the transistor scale.

CoolCube $^{\text{TM}}$  aims at processing transistors on top of each other sequentially. Its implementation faces the challenge of being able to obtain a high performance top transistor processed at sufficiently Low Temperature (LT) in order to preserve bottom FET performance.

This year several key points have been evaluated such as:

- Determination of maximum thermal budget supported by the bottom FDSOI transistor.
- Evaluation of nanosecond laser anneal as an alternative to SPER (Solid Phase Epitaxy Regrowth) for top transistor dopant activation.
- -Technological modules development such as low temperature gate stack, low-k spacer...
- Quantification of Power, Performance, Area (PPA) gain with CoolCube<sup>™</sup> integration versus planar technology for FPGA applications.

Determination of maximum thermal budget has been evaluated for advanced FDSOI technology with in-situ doped RSD (SiGe:B/ SiC:P) and SiGe channel for pMOS [1].

Various anneals have been applied after the pre-metal dielectric CMP ranging from 400°C up to 550°C, 2hours. Fig.1 shows that the transistor's performance is preserved whatever the thermal budget.

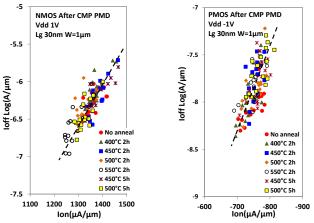


Figure 1: Determination of the maximum TB for bottom FET performance preservation. The Ion /Ioff trade-off is not degraded whatever the TB applied (up to 550°C, 2h).

Electrical analysis revealed no EOT regrowth no work function variation no junction modification. Despite a salicide

sheet resistance modification beyond 500°C, the NiPtSi salicide (NiPt with 15% Pt salicidation) presents no evidence of agglomeration. As a conclusion this technology can endure relatively high thermal budget (up to 500°C), opening new options for top FET fabrication.

One of the most critical thermal budgets in the top FET process is the dopant activation. Laser ( $\lambda$ =308nm, pulse 200ns) activation seems well adapted to 3D sequential as it enables a local annealing of the top MOSFET up to 1200°C while the temperature of the bottom one stays cool (500°C, corresponding to the temperature limit determined previously).

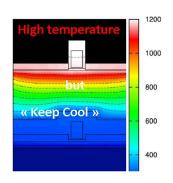
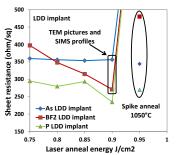


Fig.2 shows that successful RSD recrystallization has been obtained thanks to nanosecond laser anneal without melting the gate thanks to an appropriate capping. Also sheet resistance measurements shows that laser activation can largely compete with spike 1050°C anneal.



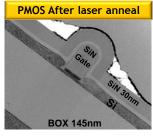


Figure 2: (left) Sheet resistance measurements for As, BF2, P versus laser anneal energy. RTA spike sheet resistance is also plotted as reference. (right) TEM cross section of a PMOS FDSOI transistor after RSD recrystallization using nanosecond laser anneal.

Finally PPA analysis on FPGA with stacked 14 nm-node-FETs shows an area reduction of 55% and Energy Delay product of 47% compared to the 14 nm node planar FDSOI integration [3]. Thus, CoolCube™ technology appears as an efficient way to pursue Moore's law in term of area and performance without resorting to transistor's scaling.

#### Related Publications:

[1] C. Fenouillet-Beranger, B. Mathieu, B. Previtali, M-P. Samson, N. Rambal, V. Benevent," New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI", *IEDM* 2014.

[2] P. Batude, M. Vinet, B. Previtali, C. Tabone, C. Xu, J. Mazurier et al., "Advances, Challenges and Opportunities in 3D CMOS Sequential Integration", IEDM 2011.

[3] O. Turkyilmaz, G. Cibrario, O. Rozeau, P. Batude, F. Clermidy, "3D FPGA using High-Density Interconnect Monolithic Integration", Design, Automation and Test in Europe Conference and Exhibition (DATE), 24-28 March 2014, Dresden, Germany.



# Very Low Temperature Deposition - Etch of SiGe:B Raised Sources and Drains for CoolCube<sup>™</sup>

#### Research topics: SOI, Monolithic 3D Integration, CMOS

J.M. Hartmann, V. Benevent, J.P. Barnes, M. Veillerot

### Partnership: STMicroelectronics, Probions Sponsorship: Nano2017

In-situ boron-doped SiGe Raised Sources and Drains (RSDs) are mandatory to thicken the access regions and lower the contact resistance of high performance p-type Metal Oxyde Semiconductor Field Effect Transistors (p-MOSFETs) built on top of Extra-Thin Silicon-On-Insulator (ET-SOI) substrates. They can also be handy in order to boost the ON current of Tunnel FETs on ET-SOI, improve the electrical performances of Omega-gate SOI Nano-Wire FETs etc. Such RSDs are typically 15-20 nm thick, with a Ge content close to 30% and a boron atomic concentration slightly higher than 1020 cm $^{-3}$ . They are usually grown at 650°C, 20Torr with a heavily chlorinated chemistry (i.e. with SiH<sub>2</sub>Cl<sub>2</sub> + GeH<sub>4</sub> + B<sub>2</sub>H<sub>6</sub> + HCl) in order to be fully selective versus SiO<sub>2</sub> (the isolation) and Si<sub>3</sub>N<sub>4</sub> (the transistor's spacers) [1].

Being able to fabricate those RSDs at lower temperatures with higher Ge contents (above 35%, typically, in order to inject higher levels of uniaxial compressive strain in the channel) and higher B concentrations (2x1020 cm<sup>-3</sup> and higher, in order to benefit from lower contact resistances) would be most interesting in future FET devices. Process temperatures less than 600°C indeed minimize the regrowth of an interfacial layer between the high-K dielectrics and the semiconducting channel and allow a better control of short channel effects. They also enable monolithic 3D integration (the so-called CoolCubeTM approach), i.e. the stacking of ET-SOI FETs one upon another thanks a sequential integration scheme. The thermal budget used for the fabrication of the top FETs has then to be low enough to preserve the stability of the silicide of the bottom FETs and retain good electrical performances. This leads to peculiar constraints concerning RSDs. Advanced Cyclic Deposition / Etch (CDE) strategies have then to be used [2-3]. The higher order silanes (gaseous Si<sub>2</sub>H<sub>6</sub>, liquid Si<sub>3</sub>H<sub>8</sub> etc...) that yield meaningful growth rates at low temperatures are indeed intrinsically non selective versus dielectrics; HCl (or Cl<sub>2</sub>) etches that remove poly- or amorphous materials on dielectrics much faster that single-crystalline SiGe:B in the sources and drains regions have then to be used to obtain the overall selectivity aimed for (see Fig.1).

We have thus leveraged our know-how on disilane-based epitaxial growth of SiGe [4] to develop an innovative CDE process for the selective deposition of heavily in-situ boron-doped SiGe:B RSDs at 500°C [5], i.e. a temperature 150°C lower than in our conventional recipe.

CDE = repetitions of growth and selective etch steps in order to obtain the required layer thickness

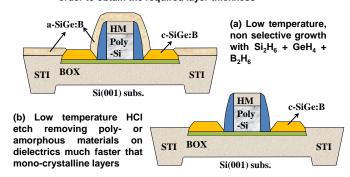


Figure 1: Schematics showing how low temperature CDE works on patterned ET-SOI wafers with gate stacks.

Rather smooth, facetted SiGe:B raised sources and drains (with no poly-SiGe:B on top of dielectrics covered surfaces anymore) were obtained in the end, as shown in Fig.2.

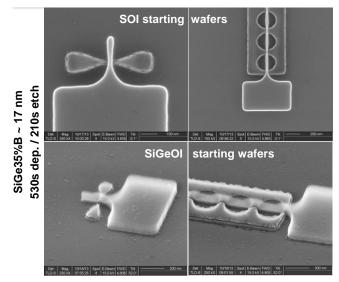


Figure 2: Top-view and 3D Scanning Electron Microscopy images of approximately 17 nm thick SiGe35%:B RSDs raised sources and drains grown at 500°C, 20 Torr thanks to on each side of ET-SOI pFET transistors.

#### Related Publications:

[1] J.M. Hartmann, V. Benevent, J.P. Barnes, M. Veillerot, D. Lafond, J.F. Damlencourt, S. Morvan, B. Prévitali, F. Andrieu, N. Loubet, D. Dutartre, "Mushroom-Free Selective Epitaxial Growth of Si, SiGe and SiGe:B Raised Sources and Drains", *Solid State Electronics*, Vol. 83, may 2013, Pages 10-17.

[2] J.M. Hartmann, V. Benevent, J.P. Barnes, M. Veillerot and C. Deguet, "Disilane-based Cyclic Deposition / Etch of Si, Si:P and Si1-yCy:P

layers Part I: the elementary process steps", Semiconductor Science and Technology, Vol. 28, No. 2, 2013.
[3] J.M. Hartmann, V. Benevent, J.P. Barnes, M. Veillerot. B. Prévitali, P. Batude, "Disilane-based Cyclic Deposition / Etch of Si, Si:P and Si1-yCy:P layers Part II: the CDE features", Semiconductor Science and Technology, Vol. 28, No. 2, 2013.

[4] J.M. Hartmann, V. Benevent, M. Veillerot, A. Halimaoui, "Potentialities of disilane for the low temperature epitaxy of intrinsic and boron-doped SiGe", *Thin Solid Films*, Vol. 557, Pages 19-26, April 2014.

[5] J.M. Hartmann, V. Benevent, A. André, C. Sirisopanaporn, M. Veillerot, M.P. Samson, S. Barraud, Z. Essa, B. Sermage, "Very Low Temperature (Cyclic) Deposition / Etch of in-situ Boron-Doped SiGe Raised Sources and Drains", ECS Journal of Solid State Science and Technology, Vol. 3, No. 11, Pages 382-390, 2014.



# Tunnel Transistors (TFET) & Single Electron Transistors (SET) in Nanowire Architecture on SOI

### Research topics: Disruptive Devices, Ultra-Low-Power, SOI, TFET, SET

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Partnership: IMEP-LAHC, Brown Univ., EPFL, Univ. of Udine, FZJ, Berkeley Sponsorship: FP7-STEEPER, FP7-TOLOP

TFET: In order to propose an energy efficient logic, we evaluate the interest of Beyond CMOS devices. Our objective is to design devices with non CMOS like switching properties to be integrated in addition to CMOS to provide better energy efficiency for computing applications. On one hand Tunneling Field Effect Transistors (TFET) performance is boosted thanks to band engineering and architecture optimization. On the other hand low-temperature conductance measurements in trigate nanowire FET are done to investigate the gate-induced addition of the first few electrons to the edges modes located in the corners of the nanowire. This localization leads to quantum dot behavior being potentially promising candidates for silicon spin qubits.

#### High drive current TFET:

We investigate the performance of planar SOI tunnel FETs in fully Depleted configuration and in nanowire architecture, for narrow band gap channel (SiGe) [1]. The studied tunneling boosters enable to increase the TFET ON state currents in n-mode and p-mode operations (which outperforms the previous TFET state-of-the-art).

The physical limit of MOSFET subthreshold slope is 2.3kT/q. With low supply voltages, this slope degrades the Ion/Ioff current ratio. Tunneling FETs (TFETs) use band-to-band tunneling (BTBT) carrier injection, TFETs subthreshold slopes are thus free from the MOSFET thermionic injection limit of 2.3kT/q (60mV/dec at room temperature). Sub-60mV/dec experimental results have already been reported, albeit in a narrow gate-bias range. Yet, experimental TFETs suffer from low Ion, with typical values under 1-10µA/µm.

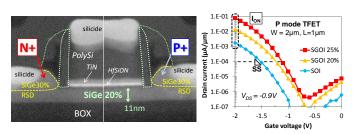


Figure 1: a) STEM picture of transistor; b) Impact of the Ge fraction in the SiGe channel on the measured Id(Vgs) characteristics.

We present for the first time strained SiGeOI 20% and 25% TFETs (co-integrated with CMOS) using SOI CMOS process featuring High-K Metal Gate.

Compressive SiGe channels with 25% Ge fraction enable to increase by a factor of 20 the saturation currents, even at small gate length (Lg=50nm).

This large gain is due to the threshold voltage shift and to enhanced intrinsic band-to-band tunneling injection (both related to the narrow band gap of SiGe channels).

We also show that both tunneling junctions (Source/channel and channel/drain) have to be considered simultaneously to explain TFET behavior correctly [1].

SET: We also investigated the onset of the few-electron regime through the undoped channel of a Si nanowire FET.

By combining low temperature transport measurements and self-consistent calculations, we revealed the formation of one-dimensional conduction modes localized at the two upper edges of the channel. Charge traps in the gate dielectric cause electron localization along these edge modes, creating elongated quantum dots with characteristic lengths of ~10nm. We observe single-electron tunneling across two such dots in parallel, specifically one in each channel edge. We identify the filling of these quantum dots with the first few electrons, measuring addition energies of a few tens of milli-electron volts and level spacings of the order of 1meV, which we ascribe to the valley orbit splitting.

The total removal of valley degeneracy leaves only a 2-fold spin degeneracy, making edge quantum dots potentially promising candidates for silicon spin qubits.

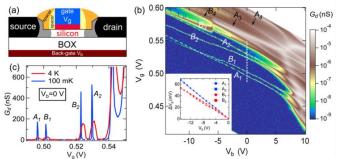


Figure 2: a) Layout of the studied sample featuring the thin intrinsic silicon channel b) Source-drain conductance versus back and front gate bias (Vb, Vg) at T=0.1K. Five isolated resonances are identified corresponding to the addition of one electron in the dots. c) A cut of the panel (b) along the white dotted line (Vb=0V) at T=0.1K and T=4.2K

#### Related Publications:

- [1] A. Villalon, G. Le Carval, S. Martinie, C. Le Royer, M.-A. Jaud, S. Cristoloveanu, "Further Insights in TFET Operation", *IEEE Transactions on Electron Devices*, Vol. 61, No. 8, August 2014, pp. 2893-2998.
- [2] B. Voisin, V.-H. Nguyen, J. Renard, X. Jehl, S. Barraud, F. Triozon, M. Vinet, I. Duchemin, Y.-M. Niquet, S. De Franceschi, M. Sanquer, "Edges-states at the onset of a silicon trigate FET", *IEEE Silicon Nanoelectronics Workshop*, Honolulu, HI, USA, 8-9 June 2014.
- [3] B. Voisin, V.-H. Nguyen, J. Renard, X. Jehl, S. Barraud, F. Triozon, M. Vinet, I. Duchemin, Y.-M. Niquet, S. De Franceschi, M. Sanquer, "Few-electron edges-states quantum dots in a silicon nanowire FET", *Nano Letters*, Vol. 14, pp. 2094-209, 2014.

### **Advanced Nanowire FET Technology**

Research topics: SOI, MOSFET, Nanowire, Strain

S. Barraud, M. Cassé, P. Nguyen, M.P. Samson, F. Glowacki, J.M. Hartmann, M. Vinet

### Partnership: IBM, STMicroelectronics, SOITEC Sponsorship: Nano2017

Nanowire (NW) transistors are today widely recognized as promising to pursue Moore's Law beyond FinFET and Fully-Depleted Silicon-On-Insulator (SOI) CMOS architectures. If aggressively scaled NW transistors have already been demonstrated, strain-induced performance enhancement in short-channel NWs still need to be better understood in N-type and P-type Field Effect Transistor (FET) nanowires. Here, a successful co-integration of hybrid Si and SiGe channels in high AC performance NW CMOS devices that outperform state-of-the-art SOI nanowires was demonstrated for the first time.

An optimized Ge enrichment process described in [1] was used in p-FET regions (n-FET regions are made of silicon) for the formation of localized SiGeOI layers. Nanowire transistors were then fabricated thanks to a top-down approach with a high-k/metal gate. Fig.1 shows cross-sectional Transmission Electron Microscopy (TEM) images of  $\Omega\text{-Gate p-FET (SiGe-channel)}$  NW transistors with a gate length and a diameter down to 15nm and 12nm, respectively. For long gate length (Lg=10 $\mu$ m), a significant hole mobility improvement is evidenced for SiGe channel NWs (+135% compared to Si) due to uniaxial compressive strain [2].

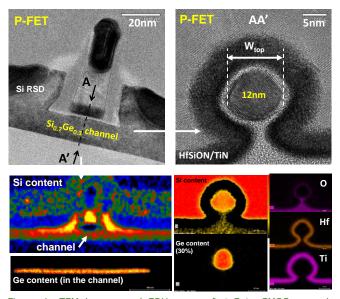


Figure 1: TEM images and EDX maps of  $\Omega$ -Gate CMOS nanowire transistors (SiGe channel for P-FET) with diameter  $\varnothing$ =12 nm and Lg=15 nm. The Ge content of the SiGe channel is close to 30% (semi-quantitative Energy Dispersive X-ray (EDX) spectroscopy).

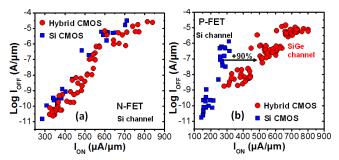


Figure 2: N-FET (a) and P-FET (b) Ioff-Ion plots showing no N-FET performance degradation. Ion=520  $\mu$ A/ $\mu$ m at Ioff=100 nA/ $\mu$ m and Vdd=0.9 V. P-FET performance is enhanced due to uniaxial compressive strain induced by the SiGe channel  $\rightarrow$  +90% Ion improvement for hybrid CMOS  $\Omega$ -Gate P-FET NWs.

For short gate length (Lg=20nm), no degradation of n-FET performance is evidenced when using a hybrid CMOS integration scheme. However, uniaxial compressive strain in p-FET SiGe-channel NWs results in a +90% Ion current improvement compared to Si devices (with Vdd=0.9 V) [2]. The uniaxial compressive strain induced by the SiGe channel improves the linear current by a factor of almost ×3 in [110] SiGe NWs with respect to [100] SiGe NWs (or Si-NWs). This was explained by valence band structure simulations in NW-FETs with the tight-binding approach. Simulations show that the compressive strain strengthens the light holes of the highest valence-subbands of [110] oriented NWs by pushing heavy holes subbands down. Precession electron diffraction with 1 nm spatial resolution has been used to measure the strain distribution in the SiGe channel. A uniaxial compressive strain was evidenced, which is in-line with the p-FET performance increase achieved with hybrid integration [2]. Ids-Vgs characteristics of the most aggressively scaled hybrid CMOS NW reported to date (with W=7 nm for p-FET and W=11 nm for n-FET with Lg down to 11 nm) with excellent electrostatic control were demonstrated. Finally, hybrid channel NW ring oscillators with 80 stages were also fabricated [2]. A 50% reduction in RO delay due to SiGechannel p-FET was evidenced.

Hybrid channel CMOS integration can thus easily be used with a high efficiency for NW-based technology.

From these results where NW have proven to be interesting to achieve low power consumption and high speed provided by the introduction of strain, next step is now to increase the current per unit area by investigating vertically-stacked silicon nanowire MOSFETs.

#### Related Publications:

[1] P. Nguyen, S. Barraud, M. Koyama, M. Cassé, F. Andrieu, C. Tabone, F. Glowacki, J.M. Hartmann, V. Maffini-Alvaro, D. Rouchon, N. Bernier, D. Lafond, M.-P. Samson, F. Allain, C. Vizioz, D. Delprat, B.Y. Nguyen, C. Mazuré, O. Faynot, M. Vinet, "High-mobility  $\Omega$ -Gate nanowire p-FET on cSGOI substrates obtained by Ge enrichment technique", *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, 06 Oct-09 Oct 2014, San Francisco, USA.

[2] P. Nguyen, S. Barraud, C. Tabone, L. Gaben, M. Cassé, F. Glowacki, J.M. Hartmann, M.-P. Samson, V. Maffini-Alvaro, C. Vizioz, N. Bernier, C. Guedj, C. Mounet, O. Rozeau, A. Toffoli, F. Allain, D. Delprat, B.Y. Nguyen, C. Mazuré, O. Faynot, M. Vinet, "Dual-channel CMOS co-integration with Si NFET and strained-SiGe PFET in nanowire device architecture featuring sub-15nm gate length", *IEDM* 2014.







Hybrid OXRAM/CBRAM: Controlling Oxygen Vacancies in Doped Oxide based CBRAM for Improved Memory Performances

Experimental and Theoretical Understanding of Conductive Bridge RAM Operations for Memory Stack Optimization

Convolutional Neural Network for Pattern Recognition Applications based on OxRAM Synapses

Insight on Low Resistance State Retention in HfO<sub>2</sub> and HfAlO based RRAM

Phase Change Memories Towards Confined Structures: Deposition Process and Phase Transformation Challenges



# Hybrid OXRAM/CBRAM: Controlling Oxygen Vacancies in Doped Oxide based CBRAM for Improved Memory Performances

#### Research topics: Resistive Memories, Non-Volatile Memories, Oxide, Copper

G. Molas, E. Vianello, M. Barci, P. Blaise, J. Guy, A. Toffoli, M. Bernard, A. Roule, F. Pierre, C. Licitra, B. De Salvo, L. Perniola

#### Partnership: ALTIS Semiconductor

CBRAM is a promising technology for future nonvolatile memories due to its good scalability, fast read and write times < 10ns. Using an oxide as electrolyte instead of chalcogenide material, CBRAM insures good high temperature retention and resistance to soldering, but at the price of higher forming voltages. In this paper the concept hybrid CBRAM assisted by oxygen vacancies is presented for the first time. We study the impact of doping the Metal Oxide resistive layer with Hf or Al in order to facilitate the Cu insertion during forming and improve the OFF resistance after RESET [1].

A Cu-based ion supply layer is deposited as a top electrode. The resistive layer was doped by co-sputtering with two types of dopants D (D being Hf or Al) with various concentrations, leading to MOx(Hf) and MOx(Al) alloys (Fig.1a). Increasing the (M+Hf)/O ratio with Hf dopants leads to a lower resistance for the fresh state, hence a lower forming voltage. With Al dopant, two antagonist effects occur: VF tends to increase as VF(Al<sub>2</sub>O<sub>3</sub>)>VF(MOx), while VF tends to be reduced as the doping content increases due to a more metallic behavior of the MOx(Al) alloy (higher (M+Al)/O ratio).

Concerning RESET, in MOx(Hf), for Vbl>1.3V a higher memory window (resulting from a higher HRS resistance) is reached in the undoped samples, while  $R_{\text{OFF}}$  saturates for doped samples. In other words, a larger memory window can be obtained in undoped samples for strong RESET conditions. On the contrary, Al doping of MOx enlarges the maximum  $R_{\text{OFF}}$  value: an optimum  $R_{\text{OFF}}$  is achieved for 10% Al doping (~3 decades increase: Fig.1b). Further increasing Al concentration starts to degrade  $R_{\text{OFF}}$  due to a too high (M+Al)/O ratio [2].

In Hf-doped samples, VSET decreases with the doping concentration due to a lower initial  $R_{\text{OFF}}$ . Interestingly, the strongly doped sample is forming free, in the sense that the forming and SET voltages are equal (Fig.1c).

Retention was then measured at  $200^{\circ}\text{C}$  for the various samples. Stable memory window was maintained after  $1\text{E}^{5}\text{s}$ , while some degradation appears at 21% Al doping content, both on LRS and HRS (Fig.1d). Summarizing, Hf dopant can be used for reducing the forming voltage; small concentration of the Al dopant can be used to improve the memory window without a huge change of the forming voltage. In both cases no major changes of switching parameters and data retention performances are observed.

Then, we studied the impact of Cu inclusion in the electrolyte. We calculated (DFT) the formation enthalpy to add a Cu atom in the resistive layer. A high energy of 3.2eV is required. Assuming oxygen vacancies in the resistive layer, the energy cost to insert Cu in interstitial site is strongly reduced (1.3eV), indicating that the formation of a

Cu filament should be easier (1.3eV). Then we show that in MOx(Hf), Cu insertion is easier than in MOx and MOx(Al), explaining the lower VF. In MOx(Hf) and MOx(Al) doped samples, inserting oxygen vacancies strongly facilitates the Cu inclusion, easing the filament formation (Fig.2). In an oxide based CBRAM, the energy cost to insert Cu atoms in the electrolyte is elevated, leading to the requirement of a forming operation. During this phase, oxygen vacancies (VO) may be created in the oxide, facilitating the Cu migration in the resistive layer. During RESET, Cu is removed but the remaining defects in the electrolyte prevent the recovery of the fresh resistance level. In doped electrolytes, Cu insertion in VO is strongly facilitated, less VO are required to form the filament. In MOx(Hf), Cu insertion is facilitated, resulting in reduced VF (dopant assisted forming). In MOx(AI), lower VO generation during forming allows reaching a higher ROFF, enhancing the window margin.

In [2,3] a phenomenological description of oxide based CBRAM is presented, elucidating the role of oxygen vacancies. Doping the electrolyte with Hf or Al respectively facilitates the Cu filament formation, reducing the forming voltage, or allows to take advantage of an alternative alloy with intrinsic improved window margin (3 decades of  $R_{\text{OFF}}/R_{\text{ON}}$  increase, stable 200°C retention) and keeping constant the operating voltages.

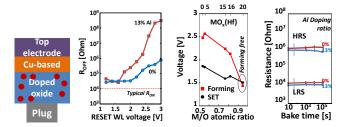


Figure 1: (a) doped electrolyte CBRAM schematic (b) RESET characteristics for various Al doping (c) SET and forming voltages as a function of Hf doping (d) retention at 200°C for Al doped CBRAM.

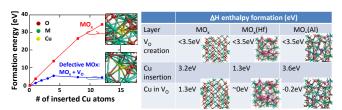


Figure 2: (left) Energy cost (DFT) to insert a Cu atom in the electrolyte; (right) Calculated formation enthalpy energy using 1st principal calculations (DFT) for various structural modifications.

#### Related Publications:

[1] G. Molas, E. Vianello, J. Guy, F. Longnos, P. Blaise, M. Barci, T. Cabout, B. Traore, G. Palma, M. Bernard, A. Roule, C. Carabasse, V. Delaye *et al.*, "Resistive RAM for non-volatile memory applications", 18<sup>th</sup> Workshop on Dielectrics in Microelectronics, Wodim 2014, 9-11 June 2014, Cork Ireland, invited paper.

[2] G. Molas, E. Vianello, F. Dahmani, M. Barci, P. Blaise, J. Guy, A. Toffoli, M. Bernard, A. Roule, F. Pierre, C. Licitra, B. De Salvo, L. Perniola, "Controling oxygen vacancies in doped oxide based CBRAM for improved memory performances", *IEDM* 2014.

[3] G. Molas, E. Vianello, L. Perniola, B. De Salvo, "Advanced Resistive memories for non-volatile applications", CMOS Emerging Technologies Research Symposium, 06-08 July 2014, Grenoble, France, invited paper.



# Experimental and Theoretical Understanding of Conductive Bridge RAM Operations for Memory Stack Optimization

### Research topics: Resistive Memories, Non-Volatile Memories, Oxide, Copper

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#### **Partnership: ALTIS Semiconductor**

Conductive Bridge RAM (CBRAM) are envisaged as a promising alternative to Flash memory due to their high speed, low voltage, low consumption and ease of integration in the back end of a logic process.

We are currently evaluating the potentiality of CBRAM memories for Flash replacement and non-volatile memory applications. To this aim we have investigated the impact of the CBRAM memory stack on the Forming, SET operations and retention performances.

Kinetic Monte Carlo simulations, based on inputs from abinitio calculations and taking into account ionic hopping and chemical reaction dynamics are used to simulate the forming process, computing the copper injection in the electrolyte from the top electrode during the filament formation. This model allows to analyze the experimental results obtained on decananometric CBRAM devices [1-2]. With this model we can propose guidelines to optimize the CBRAM stack, targeting Forming voltage reduction, improved trade-off between SET speed and disturb immunity (time voltage dilemma) and insure good retention as represented in Fig.1 and Fig.2.

Our model was used to fit the experimental forming and SET characteristics of CBRAM devices. The forming and SET time is measured as a function of the forming and SET pulse width. The so-obtained t(V) curve shows an exponential behavior. A steep curve indicates a good trade-off between short SET time and good immunity to disturb. These characteristics were fitted with our model for various technological splits, allowing to evaluate the impact of the CBRAM stack on forming and SET performances. In summary we demonstrated that:

- Playing with the top and bottom electrode work function allows to shift the t(V) curve, without changing the slope.
- Playing with the electrolyte thickness and permittivity can enhance the impact of the applied voltage and improve the SET speed and disturb immunity.

Then we have evaluated the retention performances and thermal stability of an optimized CBRAM, composed of a metal oxide electrolyte and a Cu-based top electrode. Retention characteristics were measured from room temperature up to 300°C (as shown in Fig.3), for various programming currents. We showed that the memory could remain stable for a programming current of  $100\mu A$  up to 300°C, and up to 250°C for a programming current of  $80\mu A$ . Finally we have extracted the resistance drift as a function of the programming current. High Iprog insures good low resistive state stability but degrades high resistive states. This allowed us to identify that the operating window

insuring 10 years retention at 130°C was  $30\mu A < Iprog < 125\mu A$  [3]. All these results demonstrate the strong potentiality of this memory for non-volatile memory applications.

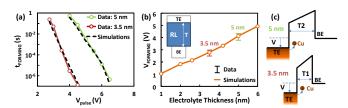


Figure 1: (a) CBRAM forming time as a function of the forming voltage for two electrolyte thicknesses. Experimental data and simulations are represented. (b) Impact of the electrolyte thickness on the forming voltage. (c) CBRAM stack band diagram showing the impact of the electrolyte thickness on the electric field in the structure.

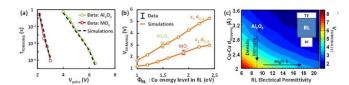


Figure 2: (a) forming time as a function of the forming voltage for two CBRAM electrolytes. (b) Impact of the Cu trap depth in the electrolyte on the forming voltage (c) Impact of the Cu-Cu hopping distance (during filament formation) and electrolyte permittivity on the forming voltage.

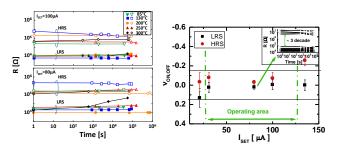


Figure 3: Retention characteristics of a metal oxide CBRAM for various temperatures and programming currents Iprog. Retention loss rate as a function of the programming current allowing to identify the operating window insuring 10 years retention at 130°C.

### Related Publications:

[1] J. Guy, G. Molas, P. Blaise, C. Carabasse, M. Bernard, A. Roule, G. Le Carval *et al.*, "Experimental and theoretical understanding of Forming, SET and RESET operations in Conductive Bridge RAM (CBRAM) for memory stack optimization", *IEDM* 2014.

[2] G. Molas, E. Vianello, L. Perniola, "Resistive RAM for non-volatile memory applications, Focus on temperature impact", *IWCMM* 2014.
[3] M. Barci, J. Guy, G. Molas, E. Vianello, A. Toffoli, J. Cluzel, A. Roule, M. Bernard, C. Sabbione, L. Perniola, B. De Salvo, "Impact of SET and RESET conditions on CBRAM high temperature data retention", *2014 IEEE International Reliability Physics Symposium, IRPS 2014*, 1-5 June 2014, Waikoloa, HI, USA.

# Convolutional Neural Network for Pattern Recognition Applications based on OxRAM Synapses

#### Research topics: OxRAM, Synapse, Neuromorphic Circuits

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Partnership: CEA-LIST, IMEP-LAHC Sponsorship: Nano2017, LabEx-MINOS

Software implementations of convolutional neural networks (CNNs) have become in recent years the first classification solutions to compete with human accuracy on tasks such as the recognition of handwritten characters, traffic signs, or people faces. State of the art software implementations of CNNs are based on the implementation of very large networks using power-hungry GPU clusters. The biggest challenge is the integration of CNNs into low-power embedded systems. Thanks to the use of HfO<sub>2</sub>-based OxRAM devices, we present a CNN architecture which implements the computation directly in memory, with the benefits of non-volatility and energy efficiency, opening the way to the implementation of CNNs in embedded systems [1]. The OxRAM devices are chosen due to their low operating current, short switching time and good endurance [2]. These aspects are necessary for effectively implementing CNNs.

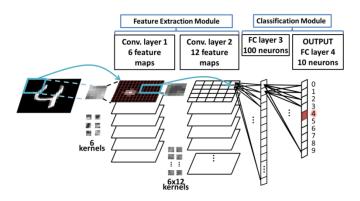


Figure 1: Schematic view of the proposed architecture for the recognition of handwritten characters.

Fig.1 shows a schematic view of the OxRAM-based CNN architecture. The CNN, is composed of a feature extraction module and a classification module. The feature extraction module is used to extract a set of kernel features from the input image that has to be classified into feature maps. This is done with convolution operations performed in two cascaded convolutional layers. Once the complex input image has been split into a set of feature maps, the classification module associates the obtained feature maps to the category which the input image belongs to, by activating the correct output neuron.

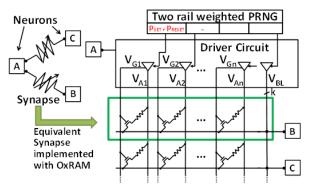


Figure 2: Circuit schematic of the OxRAM-based synaptic kernel. All OxRAM devices on the same row form an equivalent synapse. A driver circuit is used to individually program the OxRAM devices and to propagate the spike signal between neuron layers.

The circuit schematic of the OxRAM-based synapses, used to store the kernel features and perform the convolution operations, is represented in Fig.2. An equivalent synapse is obtained with the OxRAM devices on the same row of the memory array. The proposed implementation of CNN requires 10x less OxRAM synapses compared to a standard neural network. An application of image recognition on a database of 60,000 images has been demonstrated in simulation with a recognition success of 98% (Table I). The use of weak programming conditions for OxRAM devices allows to improve the energy efficiency of 85% with respect to strong programming conditions. The cost is a reduction of recognition performance of only few units percent.

	Weak programming conditions	Strong programming conditions
SET energy / device	5 pJ	34 pJ
RESET energy / device	9 pJ	58 pJ
Recognition success	94.0%	98.3%

Table I: Summary of the network performance obtained for weak programming conditions, and strong programming conditions. Using weak programming condition allows a significant reduction of the energy consumption, at the cost of a reduction of the recognition of few units percent.

#### Related Publications:

[1] D. Garbin, O. Bichler, E. Vianello, Q. Rafhay, C. Gamrat, L.Perniola et al., "Variability-tolerant Convolutional Neural Network for Pattern Recognition Applications based on OxRAM Synapses," 2014 IEEE International Electron Devices Meeting (IEDM), 2014.
[2] E. Vianello, O. Thomas, G. Molas, O. Turkyilmaz, N. Jovanovic, D. Garbin et al., "Resistive memories for ultra-low-power embedded computing design," 2014 IEEE International Electron Devices Meeting (IEDM), 2014.



# **Insight on Low Resistance State Retention** in HfO2 and HfAIO based RRAM

#### Research topics: RRAM, Simulation, Device Characterization and Modeling

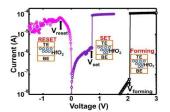
B. Traoré, T. Cabout, E. Vianello, P. Blaise, G. Molas, E. Jalaguier, H. Grampeix, L. Perniola, B. De Salvo

#### Partnership: STMicroelectronics, Stanford University Sponsorship: Nano2017, Nanosciences Foundation

Oxide based RRAMs belong to the family of two terminal devices whereby an oxide layer is fabricated between two metal electrodes and whose resistance levels can be switched between two distinct and stable states generally referred to as Low Resistance State (LRS) or Ron and High Resistance State (HRS) or Roff. LRS is attributed to the creation/reconstruction of a conductive path conductive filament (CF) while HRS is associated with the rupture of the CF. Fig.1 (left) shows typical current voltage (IV) of RRAM. Despite the simple structure of these devices, many challenging issues still remain concerning their variability and thermal stability. In this study, we looked at the low resistance state thermal stability of hafnia based RRAM as well as the impact of alloying it with Al.

First we demonstrated that the programming temperature (even if it has no influence on the initial resistance) has a strong effect on thermal stability of the conductive filament [1]. The time-dependent evolution of average of LRS resistance is shown in Fig.1 (right). Ron fails towards high resistance values as the retention time increases which we associate to the diffusion of oxygen vacancies forming the CF bottom left). Devices programmed at temperature (red curves in Fig.1 right) exhibit stronger degradation. This phenomenon is even reinforced when working at lower compliance current (i.e. dash-lines). We associate the thermal stability to the CF shape: reducing the conductive filament diameter while keeping high density of the oxygen vacancies improves data retention.

In addition to the improvement of Ron thermal stability by low SET temperature, we also looked at the impact of doping  $HfO_2$  by Al [2]. Fig.2 (left) shows that Ron retention gets improved at all the investigated temperatures with Al doping. The extracted failure times, based on the failure criteria, are plotted in an Arrhenius (Fig.2 right). Higher activation energy, Ea, is extracted for HfAIO and more than 10 years retention of 130°C and 154°C are extrapolated for the HfO<sub>2</sub> and HfAlO samples respectively. In order to have a microscopic understanding on Ron retention, we used ab



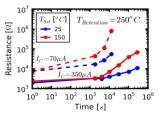


Figure 1: (a)RRAM IV plot and schematic models showing its working principle (b) High temperature data-retention at 250°C for two SET temperatures (25°C in blue, 150°C in red) and for two current compliances (continuous lines 350µA, dashed lines 70µA). The characteristics are average on 20 devices.

initio based oxygen vacancy (Vo) diffusion calculations via the Nudged Elastic Band (NEB) technique to investigate Ron retention which we associated with Vo diffusion.

To compare Vo diffusion barriers in HfO2 with and without Al doping, we constructed 2 supercells (Fig.3 top): one being pure HfO<sub>2</sub> and the other corresponding to HfO<sub>2</sub> alloyed with Al resulting in Hf<sub>1</sub>-xAl<sub>2</sub>xO<sub>2</sub>+x stoichiometry (HfAlO). The results show that Vo diffusion barrier in HfAlO is higher than in pure  $HfO_2$  (Fig.3 bottom right). This is in agreement with the experimental data showing better Ron retention for HfAlO compared with HfO<sub>2</sub>. The study provides a microscopic insight on Ron retention improvement in HfAlO via a simple explanation based on its higher atomic density (atoms/cm³) associated with shorter bond lengths between cations and anions in the presence of Al.

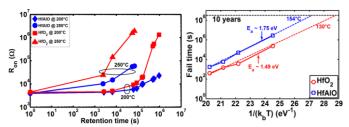


Figure 2: (left) Improvement of Ron retention with Al doping. (right) Arrhenius plot showing good retention over ten years for both.

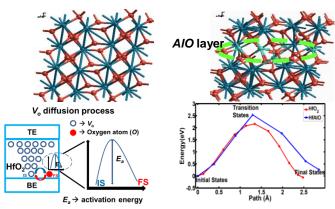


Figure 3: (top left): Atomistic structures of HfO2 and (top right): HfAlO used for ab initio calculations. (Bottom left): Figure 13. Model showing Vo diffusion process during Ron retention where the CF ruptures at the tip (constriction). The diffusion process is associated with an Ea that is calculated with the NEB technique. (Bottom right) High diffusion barrier for Vo in HfAIO calculated with ab initio methods in agreement with experiment of (Fig.2 right).

#### Related Publications:

[1] T. Cabout, E. Vianello, E. Jalaguier et al. "Effect of SET temperature on data retention performances of HfO2-based RRAM cells", 2014 IEEE 6<sup>th</sup> International Memory Workshop (IMW), 18-21 May 2014, Taipei.
[2] B. Traoré, P. Blaise, E. Vianello *et al*. "Microscopic understanding of the low resistance state retention in HfO2 and HfAlO based RRAM",

2014 IEEE International Electron Devices Meeting (IEDM), 2014.



# **Phase Change Memories Towards Confined Structures: Deposition Process and Phase Transformation Challenges**

## Research topics: Phase-Change Memory, PCM Material Confinement

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## Partnership: CNRS-LTM<sup>1</sup>, CNRS-LNCMI<sup>2</sup>, ALTATECH Sponsorship: LabEx-MINOS, RTRA-Percevall, Minalogic-PRECINOV

Among the emerging nonvolatile memory technologies, phase change random access memory (PCRAM) is considered to be one of the most promising technology thanks to its unique set of features such as high scalability, multi-level storage capability, good data retention and endurance. However, the high power consumption during the RESET operation is a major obstacle for this technology and must be reduced in order to compete with the current Flash memory technology. The integration of the phase change material (PCM) into high aspect ratio lithographic structures can lead to reduced RESET currents by improved thermal confinement. Thus, a highly conformal deposition process is mandatory. In that context a Plasma Enhanced Metal Organic Chemical Vapor Deposition (PE-MOCVD) process for the deposition of GeTe and GeSbTe PCMs was developed in CEA-Leti on the ALTACVD200, an alpha tool supplied by Altatech Company. Contrary to atomic layer deposition (ALD) where the GST composition range is very tight, various compositions of amorphous Ge-Sb-Te layers can be deposited by PECVD using commercial organometallic precursors TDMA-Ge, TDMA-Sb and DIP-Te. Various film stoichiometry can be obtained thanks to the pulsed injection system of liquid precursors allowing to control films stoichiometry, which results in a mastering of the PCM films characteristics. Amorphous and smooth GeTe layers were successfully deposited on Si, SiO<sub>2</sub>, SiN and TiN substrates. By tuning plasma parameters, we were able to reduce the C contamination induced by the M-O precursors in GeTe films from 20 to 5 at. % [1]. The first electrical behavior characterization of GeTe deposited with such process and integrated in a planar PCRAM memory cell is shown in Fig.1a.

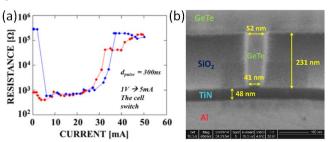


Figure 1: (a) SET to RESET and RESET to SET transitions for a GeTe film deposited by PE-MOCVD and integrated in a mushroom-type memory cell. Resistance is plotted against programming current. (b) Cross section SEM image of a 50 nm SiO2 via which have been filled with GeTe by PE-MOCVD with DF plasma.

By using a Dual Frequency mode (DF) GeTe films could be successfully deposited in 50 nm SiO<sub>2</sub> via (Fig.1b) with a Tshape: the gap is perfectly filled and the top is covered by a smooth and homogenous layer. No void or any recess is observed; furthermore CMP is not necessary, PCM is ready to be integrated in the final memory device thanks to plasma DF mode.

Thus, PE-MOCVD is a promising route to achieve the deposition of PCM in confined structures for the future PCRAM applications.

But such structures open tremendous questions regarding the impact of geometrical confinement and ultimate scaling of PCM on its phase change properties. In that context we have studied the impact of the nature of interfaces on the crystallization of thin and ultra-thin PCM films. All our results suggest that the crystallization mechanisms of PCM films is highly dependent on the nature of their cladding layers. As an example, in GeTe and GST thin films interfaced with Ta layers, the PCM crystallization temperature  $T_x$  is significantly higher compared to values reported in literature for films capped with  $SiO_2$  [2]. This effect is present in 100 nm thick films. Such a remarkable difference in Tx, only due to an interface effect, was never reported before. Our synchrotronbased X-ray diffraction investigations revealed that PCM films which crystallize at high T exhibit no crystalline texture (Fig.2b) compared to highly textured films crystallizing at low T (Fig.2a). The suppression of heterogeneous nucleation at the interfaces could also explain this spectacular increase of the PCM T<sub>x</sub> (of more than 50°C in case of GeTe) considering that homogenous nucleation is typically much slower than heterogeneous nucleation, the nucleation barrier  $\Delta G^*$  in a uniform substance being much higher than at a surface.

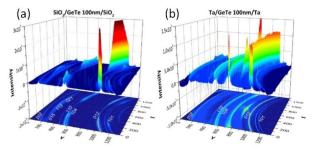


Figure 2 : 2D images of the diffracted intensity for crystallized GeTe 100 nm thick films interfaced with (a) SiO2 and (b) Ta. The GeTe phase in the SiO2 interfaced film is strongly textured, with nearly no diffracted intensity along the line X=620. In the Ta interfaced film, the GeTe phase is almost not textured. The strongly textured rings in (b) between the 012 and 104 GeTe rings are due to the Ta layers.

From a more general point of view, design of PCM cells should take these features into account. Many efforts are currently devoted to increase the T<sub>x</sub> of PCM and the memory cell retention, either by doping the PCM or modifying its composition. The use of proper interface material could be an interesting alternative, allowing to increase  $T_x$  and the retention of already optimized materials without changing t heir composition and hence keeping their best intrinsic properties such as their transformation speed, cyclability or resistance drift.

#### Related Publications:

[1] M. Aoukar, C. Vallée, D. Jourde, P. Michallon, P. Noé, "Deposition of Conformal GeTe Films by Plasma Enhanced Chemical Vapor Deposition for Phase Change Memory", 2014 MRS Spring Meeting, 21-25 April 2014, San Francisco, USA.
[2] G. E. Ghezzi, P. Noé, M. Marra, C. Sabbione, F. Fillot, N. Bernier, J. Ferrand, S. Maîtrejean, F. Hippert, "The effect of Ta interface on the

crystallisation of amorphous phase change material thin films", Applied Physics Letters, Vol.104, Issue22, id.221605, June 2014.





Block Copolymers Directed Self Assembly for CMOS Application
DSA Integration Challenges for Contact Hole & Via Patterning
Data Preparation and Electron Beam Lithography for Photonic Application
Precise Silicon Nitride Spacer Etching Using Self Limited
Light Ion Implantation
Mask-Less Lithography for Advanced CMOS Technology
Material Characterization for NanoImprint Lithography Process Simulation



# **Block Copolymers Directed Self Assembly for CMOS Applications**

# Research topics: Self-Assembly, Block-Copolymers, Advanced Lithography

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Partnership: ARKEMA<sup>1</sup>, CNRS-LCPO<sup>2</sup>, CNRS-SIMAP<sup>3</sup> Sponsorship: ARKEMA, FP7-COLISA, ENIAC-PLACYD

Block-copolymers (BCP) self-assembly has been identified as an complementary approach to conventional lithographic techniques in order to further decrease accessible dimensions for microelectronic [1,2]. However, the selfassembly properties are intimately linked to the chemical nature and architecture of the BCP material.

In 2014, CEA-Leti presented advanced progresses in Block Copolymer material development and associated characterization. Used in conjunction with "conventional" lithography, these systems lead to long-range ordered structures by combining both high density and sub-20nm

Recently CEA-Leti's industrial partner Arkema showed that PS-b-PMMA copolymers systems can be produced efficiently at the industrial scale to fulfill the future needs of microelectronic [1]. We demonstrated that PS-b-PMMA polymer natural period can be tuned down to 23nm, as depicted in Fig.1-A. Further CDs scaling down can be achieved with "high chi" materials. In collaboration with Arkema and LCPO, high resolution has been demonstrated by using a new BCP chemistry: PLA-b-PMMA. An example of this polymer with a natural period of  $L_0 = 18$ nm is reported in Fig.1-B [2].

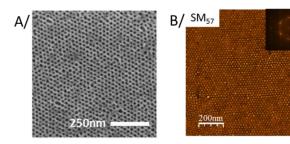


Figure 1: SEM pictures illustrating perpendicular self-assembly for A/ high resolution PS-b-PMMA polymer (LO = 23nm) [3] and B/ a PLAb-PDMS high chi BCP ( $L_0 = 18$ nm) [2].

A successful control on both period and morphology can be obtained by blending block copolymers. The self-assemblies of the blends present interesting characteristics, such as defect-free self-organization with thicker film thicknesses, as compared to pure BCPs [1]. We have also highlighted that these blends and pure BCPs share at least the same process-window for the contact shrink DSA process flow as depicted in Fig.2.

	Guiding pattern				« <u>Pure C34</u> » L <sub>0</sub> ~ 34.0nm				« <u>Blend C34</u> » L <sub>0</sub> = 34.0nm			
	0	0	0	0	•	0	0	0	0	•	0	•
	0	0	0	0	(1)	•	0	0	0	0	0	•
	0	0	0	0	0	•	0	0	•	•	<b>①</b>	0
	0	0	0	0	0	0	0	0	•	0	•	•
Mean (nm)	47.2			20.0				20.2				
3s (nm)	2.5				0.9			0.8				
Missing contacts					0			0				

Figure 2: CD-SEM images and related critical dimensions measured on 300mm wafers processed with both pure and blended BCP [1].

Moreover, fundamental understanding of self-assembly process is capital in material development and allows process optimization and order control. We demonstrated that long range order in thin films of block copolymers could be monitored by using Grazing-incidence small-angle scattering (GISAXS) techniques. In Fig.3 are reported GISAXS patterns for BCP films self-assembled jointly on the line grating (B/) and on a neighbor un-patterned area (A/). The 11 ray is missing for the guided BCP, confirming the formation of a zero defect macroscopic crystal and long range order when grapho-epitaxy approached is used.

Combining fundamental studies and R&D, CEA-Leti in relationship with Arkema put in place a unique working environment that aims to secure the technology take-off of DSA lithography for sub-10nm CMOS technology node.

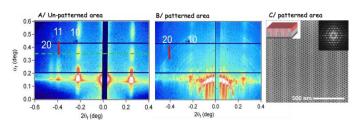


Figure 3: GISAXS results for a PS-b-PMMA polymer with cylindrical morphology on A/unpatented surface and B/patterned surface using line grid guiding patterns as illustrated on C/ [4].

#### Related Publications:

[1] X. Chevalier et al., "Improvements of self-assembly properties via homopolymer addition or block-copolymer blends", Proc. SPIE 9049,

Alternative Lithographic Technologies VI, 90490T (2014).

[2] C. Reboul *et al.*, "Self-assembly of Si-containing block copolymers with high-segregation strength: toward sub-10nm features in directed self-assembly", *Proc. SPIE* 9049, Alternative Lithographic Technologies VI, 904925 (2014).

[3] X.Chevalier *et al.*, "Self-assembly of high-resolutions PS-b-PMMA block-copolymers: processes capabilities and integration on 300mm

track", Proc. SPIE 9049, Alternative Lithographic Technologies VI, 90490Y (2014).

[4] M.Maret et al., "Probing Self-Assembly of Cylindrical Morphology Block Copolymer Using in Situ and ex Situ Grazing Incidence Small-Angle X-ray Scattering: The Attractive Case of Graphoepitaxy", Macromolecules, 2014, 47 (20), pp 7221–7229.



# **DSA Integration Challenges for Contact Hole & Via Patterning**

# Research topics: Lithography & Etching, Directed Self-Assembly, Block-Copolymers

R. Tiron, A. Gharbi, M. Argoud, P. Pimenta-Barros, I. Servin, G. Chamiot-Maitral, A. Sarrazin, K. Jullian, P. Essomba, C. Lapeyre, X. Chevalier<sup>1</sup>, C. Nicolet<sup>1</sup>, C. Navarro<sup>1</sup>

## Partnership: ARKEMA<sup>1</sup>, STMicroelectronics, SOKUDO, TEL Sponsorship: ARKEMA, STMicroelectronics, FP7-COLISA, ENIAC-PLACYD

Thanks to the intrinsic high-resolution of block copolymers (BCPs) associated with simple and low-cost processes, Directed Self-Assembly (DSA) comes out today as a promising patterning technique foreseen to be used for advanced lithography for sub-10nm technological nodes. The article summarizes the 2014 achievements on Leti's DSA works and especially highlights its potential to be considered as a manufacturing solution for advanced CMOS circuits. The work is performed on a DSA-dedicated 300mm pilot line available at CEA-Leti using Arkema's microelectronics grade BCP materials with the support of STMicroelectronics.

First, to confirm the first step maturity of DSA for high volume manufacturing, the stability of the BCP self-assembly process was studied over time. A 300mm baseline process monitoring was implemented with a 35nm-period polystyrene-b-polymethylmethacrylate (PS-b-PMMA) BCP self-assembled on unpatterned surface. Several key parameters are regularly controlled such as copolymer thickness, BCP period and CD uniformity at different steps of the process [1,2]. Statistical analysis results demonstrated that +/-4% specification is respected for all parameters. For example, Fig.1 shows the measured BCP period variation as function of weeks; in this case +/-1% variation was reached.

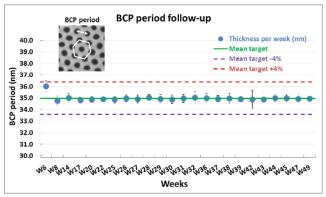


Figure 1: BCP period follow-up through time. Specification +/-4% is respected.

In CEA-Leti pilot line, the primary application of DSA was mainly focused to pattern self-aligned contact holes (CHs) using PS-b-PMMA BCP. We used the so-called graphoepitaxy approach where BCP is self-assembled inside hard mask guiding patterns predefined by conventional lithography [3]. Based on statistical analysis of defectivity and CD uniformity measurement after DSA, process windows (PWs) of CH shrink (hole-in-hole structure) are experimentally determined as function of guiding pattern dimensions for

different BCP molecular weights (corresponding to different BCP periods). These PWs enable to identify the suitable BCP molecular weight and the best guiding CD ranges required for CH patterning by DSA. As example, Fig.2 shows the CD and hole open yield (HOY) variations after DSA process as function of the guiding pattern CD using a 35nm-period PS-b-PMMA BCP. According to this graph, the corresponding PW of CH shrink (region (b)) is defined at [47nm;57nm] guiding CD range within which a 100% HOY is achieved. Inside this PW, the DSA CD variation is less than 2nm, showing that DSA can absorbs high guiding CD variation. Outside the PW, the defectivity becomes critical with missed or multiplied contacts (regions (a) and (c)).

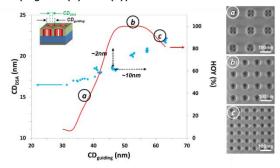


Figure 2: DSA hole CD (markers) and open yield (curve) variations as function of guiding pattern CD after CH shrink using a 35nm-period BCP.

Finally, etching transfer of DSA patterns was also demonstrated into typical MEOL and BEOL stacks of CMOS via patterning [4]. Good CD uniformity and high pattern fidelity are obtained as shown in Fig.3.

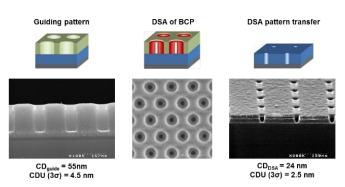


Figure 3: Schematic representation and associated SEM images of CH shrink integration at different steps of DSA process.

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- [3] A. Gharbi et al., " Contact holes patterning by directed self-assembly of block copolymers: What would be the Bossung plot?", Proc. SPIE 9049, Alternative Litho. Techno. VI, 90491N (2014).
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# Data Preparation and Electron Beam Lithography for Photonic Application

## Research topics: E-beam Lithography, Photonic, Data Preparation

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Partnership: ASELTA, VISTEC Electron Beam Lithography Group Sponsorship: IRT Nanoelec.

Electron Beam (e-beam) lithography enables flexibility, fast short-loop developments and high-resolution patterning which make this technique interesting for Silicon Photonics developments. Prior to the lithography process step, the ebeam Proximity Effect Correction (PEC) for photonics consists in fracturing the design and defining the proper doses. The fracturing was adapted to the shots allowed by the VISTEC Variable Shaped Beam (VSB) tool installed inside CEA-Leti premises: size-limited rectangles (0 and 45°) and triangles as well. In this way, the correction is more robust (no post-fracturing is performed by the VSB tool) and the exposure time which is closely related to the number of shots can be quickly estimated. The patterning of photonics designs has to fulfill specific dimension and Line Edge Roughness (LER) requirements. The LER has to be sufficiently low to avoid power losses and malfunctions of photonics devices. In order to minimize the LER, the fractured design has to be the closest as possible from the original target, which imposes a large number of shots (see Fig.2). As a drawback, the exposure time is increasing with the number of shots. The fracturing strategy becomes a real tradeoff between the resolution and the throughput and then has to be optimized [1]. The use of high-sensitive e-beam resists significantly improves the throughput by decreasing the exposure dose together with the total number of shots. In addition, for large exposed areas, we employed larger shots of 2.4 microns x 2.4 microns (Fill Patterns) to further reduce the writing time.

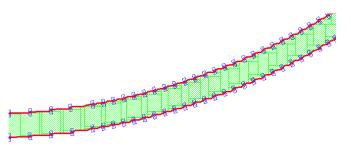


Figure 1: Fractured photonics wave guide with the resulting simulation in red and the metrology points in blue.

The dose assignment in the correction is based on a lithography model. This model is calibrated by successively exposing a dedicated layout of calibration and analyzing a set of different CD-SEM images. The model is considered to be well calibrated once the patterning of both dense and isolated patterns designed with the smallest targeted

dimensions/pitches is properly performed. Once the model is calibrated, it can be used for different photonic projects as long as the stack and tool conditions remain the same. Moreover, photoresist processes were especially optimized to improve line edge roughness (LER), pattern definition, and critical dimension (CD) homogeneities on full 8" and 12" wafers [2], which are main critical parameters for Photonics.

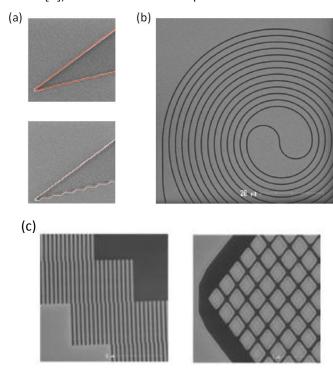


Figure 2: (a) SEM images of a tip structure patterned by our e-beam VSB equipment at CEA-Leti with (top) and without (bottom) optimizing the fracturing. The red curve shows the simulated contour. (b) Typical curvilinear photonic structure (c) Other typical photonic patterns.

In conclusion, we succeeded in patterning photonic circuits on our VSB tool at CEA-Leti with high throughput and low Line Edge Roughness (Fig.1). These achievements were possible by optimizing in advance the fracturing and by patterning on highly sensitive e-beam resists with an overdose strategy.

#### Related Publications:

[1] C. Browning, T. Quaglio, T. Figueiro, S. Pauliac, J. Belledent, A. Fay, J. Bustos, J-C Marusic, P. Schiavone, "Photonic curvilinear data processing", *Proc. SPIE* 9235, Photomask technology 2014, 92350V (2014).

[2] C. Sciancalepore, R.J. Lycett, J.A. Dallery, S. Pauliac, K. Hassan, J. Harduin, H. Duprez, U. Weidenmueller, D.F.G. Gallagher, S. Menezo, B. Ben Bakir, "Low-Crosstalk Fabrication-Insensitive Echelle Grating Demultiplexers on Silicon-on-Insulator", *IEEE Photonics Technology Letters*, Vol.27, Issue: 5, Page(s): 494-497, 2015.



# Precise Silicon Nitride Spacer Etching Using Self Limited Light Ion Implantation

#### Research topics: Atomic Layer Etching, Implantation, FDSOI, Spacer

#### N. Posseme, C. Arvet, O. Pollet, S. Barnola

Today, the silicon nitride spacer etching is considered as one of the most challenging step in the high performance Fully Depleted Silicon On Insulator (FDSOI) devices realization. A trade-off has to be found between silicon germanium (or silicon) recess, foot formation and nitride spacer faceting on top of the hard mask (as shown in Fig.1) directly impacting the device performances. Lowering electron temperature (low Te) or pulsing the plasma (synchronized or bias) are proposed today as solutions, presenting different advantages and drawbacks.

SiN (a)
Poly-Si
(c)
SiGe
SiO<sub>2</sub>

Figure 1: Illustration of silicon nitride spacer issues during etching: (a) Corner faceting, (b) Silicon Germanium Recess, (c) foot formation.

In a recent study, we proposed a new etch approach [1,2] to overcome these issues and meet the highly complex requirements imposed by device fabrication processes. This new etching process is based on two steps. In a first step, the film is modified in volume by a  $H_2$  or He plasma performed in a conventional etch tool (ICP or RIE) followed in a second step by a 1%HF wet cleaning with respect to remove the modified layer selectively to the non-modified materials (SiN, Si or SiGe) (Fig.2).

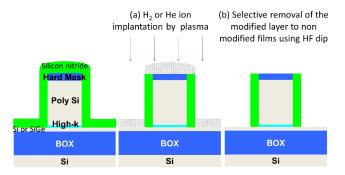


Figure 2: Description of nitride spacer etching using the new approach based on two steps:  $H_2$  or  $H_2$  or  $H_3$  or  $H_4$  of  $H_4$  in to remove the modified layer selectively to the non-modified films (b).

The etch mechanism is based on the fact that after Hydrogen or Helium plasma exposure, higher Hydrogen dose is

implanted in the silicon nitride film. This leads to the higher sensitivity to HF dip with respect to the pristine silicon nitride.

Using the new etch approach, the thickness of the silicon nitride film modification can be adjusted by tuning Hydrogen or Helium plasma operating conditions such as ion energy and processing time, impacting the ion depth penetration and the ion dose implanted in the film, respectively. This last parameter is critical since there is an ion implanted dose threshold from which the layer is enough modified to be etched by the HF dip [1].

The interest of this alternative etch process has been demonstrated on patterned wafers where the silicon nitride (9nm, deposited by PE-ALD - Plasma Enhanced Atomic Layer Deposition) must stop on Silicon Germanium (which is most critical than Si in term of damage/consumption). The Hydrogen or Helium ion implantation conditions have been adjusted to target 13.5nm silicon nitride film removal, corresponding to 50% over-etch. After silicon nitride film modification by  $\rm H_2$  ion implantation followed by 60s 1%HF dip (to remove the modified layer) the SiGe recess is less than 6A (similar results is observed when using He plasma), as shown Fig.3a.

After spacer etching, a pre clean step (30s 0.3% HF) is performed, followed without waiting time by a 10nm Silicon Germanium epitaxial growth. Fig.3b shows that the Silicon Germanium interface presents no defects after Helium processes (similar results is observed for  $\rm H_2$  plasma) which is characteristic of a good epitaxial growth. Furthermore Fig.3b shows that after epitaxial step, no foot formation is observed.

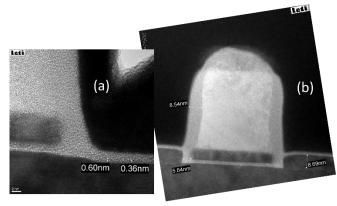


Figure 3: TEM pictures after silicon nitride etching using H2 plasma (a) or He plasma followed by an SiGe epitaxial growth (b), respectively.

Based on this description, this alternative etching approach brings new opportunities in the field of etching in terms of precise control of the film damage. Indeed the depth and profile of the ion implantation are tuned by playing on the operating conditions, allowing a precise control of the profile film modification. With this process no reactive layers are formed presenting a good compatibility with epitaxial step.

<sup>[1]</sup> N. Posseme, O. Pollet, S.Barnola, "Alternative process for thin layer etching: application to nitride spacer etching stopping on silicon germanium", Applied Physics Letters, Volume 105, Issue 5, id.051605, 2014.

<sup>[2]</sup> N. Posseme, G. Santini, O. Pollet, C. Arvet, S. Barnola, "Alternative process for thin layer etching: Application to nitride spacer stopping on Silicon Germanium", AVS 61<sup>th</sup> International Symposium and Exhibition, Nov 9-14, 2014, Baltimore, USA.



# Mask-Less Lithography for Advanced CMOS Technology

# Research topics: Advanced Lithography, Data Preparation, Resist Outgassing

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Partnership: MAPPER Lithography, TSMC, STMicroelectronics, NISSAN Chemical, Nanographics, Mentor Graphics, SOKUDO, TEL Sponsorship: IMAGINE Program

With the recurrent introduction delay of EUV lithography for High Volume Manufacturing and its constant increasing cost of ownership, mask less lithography (MLL) remains a credible alternative to answer to CMOS manufacturing industry expectations thanks to its cost attractiveness, its intrinsic resolution capability and the high-throughput of the massively parallel writing concept. Since 2009 inside the collaborative program IMAGINE, CEA-Leti works with MAPPER Lithography to push the insertion of the Mask Less Lithography approach.

After technology demonstration achieved on the pre-alpha tool at CEA-Leti, Mapper lithography introduced a new preproduction 300mm technological platform compatible with CMOS 28/20/14 nm technologies (Fig.1 & 2).



Figure 1: Picture of first MLL cluster in CEA-Leti clean room.

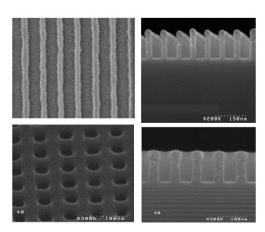


Figure 2: Top View and Cross-section of 32nm HP pattern printed with 5keV Mas Less Lithography.

First printing results are now available on the first lithography cluster installed in CEA-Leti clean room. This equipment is now using a so-called static blanker. CEA-Leti and Mapper were able to demonstrate that MLL is able to print a complete 300mm wafer in 1 hour independently of the design [1].

CEA-Leti was able to etch and to transfer in Spin On Carbon material the resist film for 32nm HP processes. The wafer was exposed with 5keV lithography prototype tool. Some etch transfer examples are presented in Fig.2.

Some extensive works have been driven and are continuously performed to better understand the Line Width Roughness root causes due to the interaction between electron and matters and potentially induced by the chemical amplified resist behavior. This work was already concretized through article in important proceeding [2].

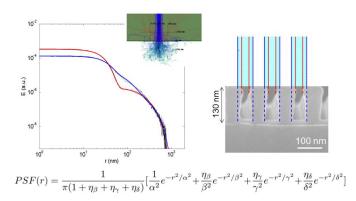


Figure 3: Simulation electron interaction with resist for thick resist application.

Complementary to the assessment of the MAPPER lithography platform, CEA-Leti drove extensive works to characterize and understand the outgassing of resist under 5kV electron beam bombardment and its associated contamination impact on the electronic optics with exposure conditions similar to a MAPPER production tool [3,4].

As conclusion, CEA-Leti is setting-up all the required infrastructures for the insertion of Mask Less Lithography for advanced node technology.

#### Related Publications:

[1] L. Lattard, "Maskless Lithography for Volume Manufacturing", SEMICON Europa, Oct. 7-9 2014, Grenoble, France.
[2] F. Delachat, C. Contancias, et al., "Determination of spot size and acid diffusion length in positive chemically amplified resist for e-beam lithography at 100 and 5keV", Journal Vacuum Science & Technology B, Vol. 32, Issue 6, 06FJ02, 2014.

[3] M.L. Pourteau, "Carbonaceous contamination growth induced by resist outgassing under e-beam exposure", Journal Vacuum Science & Technology B, Vol. 32, Issue 6, 06FB01, 2014.

[4] J.C. Marusic et al., "Assessment of carbon layer growth induced by resists outgassing in multi e-beams lithography", Proc. SPIE 9235, Photomask Technology 2014, vol. 9235, 2014.



# Material Characterization for NanoImprint Lithography **Process Simulation**

## Research topics: NanoImprint Lithography, Process Simulation

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Partnership: CNRS-SIMaP-EPM Sponsorship: ANR-METALIGAN, FP7-NAPANIL

NanoImprint lithography (NIL) is a patterning technique, sub-10-nm spatial resolution, 3D manufacturing, large scale patterning. This represents a great interest for the cost-efficient manufacturing of hard disk drives, photonic devices, high-efficiency large-area photovoltaic, and integrated circuits. In spite of the many advantages related to this technology, many challenges regarding the process simulation are still unsolved [1]. An accurate knowledge of the mechanical properties of polymers at the nanoscale, such as the material viscosity or the viscoelastic modulus, is a key step towards relevant simulations of NIL processes. However, a general, low-cost and fast method is still lacking to measure the mechanical properties of polymer melts. In CEA-Leti, we developed such a method based on the surface leveling (Fig.1) of a pattern that was manufactured with NanoImprint lithography [2]. The specific designs of the pattern we used are all patented.

Because of the extremely small length scales involved, a classical approach to extract the velocity field of the flow, such as micro-PIV, is not relevant here. As a matter of fact, the latter consists in following submicron fluorescent beads as embedded tracers in the material. Although 25nm fluorescent tracers are now available (for the smallest), this size of bead still makes the method highly invasive for sub-100 nm film flows. The general method implemented in this work is based on the characterization of the free interface of the flow (Fig.1 left). Indeed, if the motion of the free surface is known, with use of an appropriate model, we can extract some information about the flow inside the fluid. We benefit from the fact that polymers have a solid like behavior at room temperature. By a series of annealings and quenches of the resist, we could then observe a time sampling of the flow. This method allows the observation of the free interface to be made by common microscopy techniques, in this case AFM.

The leveling of the topography of a thin film can be then modeled by a capillary wave approach. In this theory, the topography of the film is expanded in terms of surface waves. Under the assumption of no slip at the bottom interface and when surface tension is the only driving force, the leveling dynamics is constrained by a dispersion relation (in Fourier space). In other words, this is a necessary condition that binds the wave vector k and the complex frequency w.

Starting from this approach many materials Maxwell (Newtonian or viscoelastic model) implemented to extract the material parameters such as the Newtonian viscosity and the terminal relaxation time [3] of coated polymer films for sub 100 nm film thickness (Fig.2).

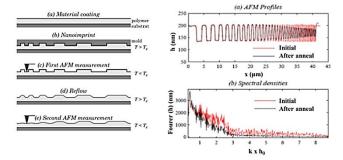


Figure 1: (Left) Main steps of the viscosity measurement method (Right) Single temperature measurement example from a line array reflows. Polystyrene (Mw = 130kg/mol) was annealed at Tg +40°C during 30s. (a) AFM measurements of the imprinted profile before and after annealing. (b) Fourier transforms of the AFM profiles.

Our results revealed that the long-wave part of the spatial spectral density, in other word general shapes and largest features of the pattern, experience a viscous, Newtonian flow. On the contrary, the short-wave part of the spectral density (shortest features, edges and corners) exhibits elastic relaxation. The transition between the two regimes is located around a critical wavelength that depends on surface tension, on the elastic plateau modulus, and on the film thickness (only for ultra-thin films). Thanks to this new material characterization method at nanoscale, a complete and reliable toolkit for NIL process simulation is now feasible. CEA-Leti is currently working on such approach to make easier and faster the adoption of this technology in industrial environment.

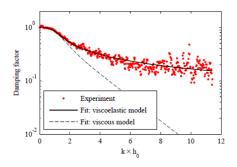


Figure 2: Damping factor of the feature height as a function of the normalized wave vector. Experimental points are fitted with two models: a purely viscous model (tx = 0) and a viscoelastic single mode Maxwell model.

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  [3] E. Rognin, S. Landis, L. Davoust, "Viscoelastic leveling of annealed thinpolystyrene films", *Langmuir*, American Chemical Society, 2014,
- 30 23), pp. 6963-6969.







3D Packaging for Vertical Power Devices

High Efficiency Multijunction Solar Cells for Concentrated PhotoVoltaics

Flexible Composites of Thermal Shape Memory Alloys and Piezoelectric Organic Materials

**Advanced Electrode Materials for Microbatteries** 



# **3D Packaging for Vertical Power Devices**

#### Research topics: Packaging, 3D, Power Devices, Bonding

J. Widiez, B. Letowski, P. Gondcharton, B. Imbert, L. Benaissa, N. Rouger, J.C. Crébier (G2ELab), T. Signamarcheix

#### Partnership: G2ELab

In the last years, many investigations have been conducted towards the development of new generation of interleaved power converters leading to reduced filtering ratings and significant savings in terms of space, volume and cost (Fig.1). However, these converters require an extended amount of active power devices making their implementation and reliability critical issues for their market and application spread. Further investigations and breakthroughs on power module integrating multiple active devices but also control signal units may offer the opportunity to improve the reliability and to simplify their implementation. In such ways, working on the assembly of power devices at wafer level is a logical research path (Fig.1).

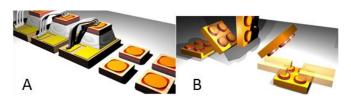


Figure 1: A. Schematic of the classical packaging approach: the vertical devices are diced, individually assembled and interconnected in a module integration approach relying on numerous soldered and bonding interfaces. B. 3D packaging approach: two matrices of vertical power devices are diced, and then assembled in 3D with a direct bonding at each interface.

Taking benefits from the possibilities offered by deep trenches isolation techniques and by wafer level packaging (using direct bonding technology), a novel 3D packaging approach is hereby introduced. A process flow that entails transferring at wafer level diodes and transistors (VMOS) onto a metallic substrate was developed. The process starts with the bonding of the active silicon layer onto a temporary substrate. So the vertical device can be processed and thinned down to an optimized thickness with respect to desired voltage breakdown. Finally the fabricated device is bonded to a metallic substrate using copper deposited layers. First results were obtained with Mo and W bulk substrates. We recently demonstrate successful power devices transfer on copper bulk substrate (Fig.2). We changed our process using in-situ pressure and annealing during the bonding step to obtain defect free bonding.

After fabrication and transfer on a metallic substrate at wafer level, identical matrices of devices are diced and prepared for the 3D assembly and interconnections (Fig.3A). The lead frame in Copper is polished to obtain a surface flat enough to be bonded using a thermo-compression technique. The surface roughness before treatment (RMS=1.3µm) is drastically reduced after planarization (RMS=1.65nm) (Fig.3right). This polishing step is realized on both surfaces of the frame. It makes possible the Cu/Cu bonding of the power

transistors on the metallic substrate on the high side of the frame and the Cu/Cu bonding of the diodes on the metallic substrate on the Low side. Either the full assembly is realized at this stage or it can be carried out in two steps, depending on the handling complexity.

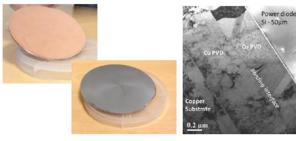


Figure 2: Successful direct bonding of a thinned Silicon wafer on a 4" bulk Cu substrate. Left: pictures of back- side (4" Cu bulk) and topside (Si power diodes before DRIE) Right: TEM image of the bonded

An underfill is inserted in order to guarantee the electrical passivation of the module, and eventually to fill up the deep trenches with a dielectric material if it has not been done at wafer level. Double side cooling can be implemented to ease the heat extraction (Fig.3D).

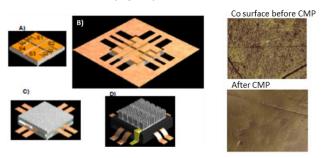


Figure 3: Right - 3D module assembly successive steps, after dicing two matrices of power devices. Left - Optical interferometer measurements of the power lead frame before and after preparation.

A novel 3D packaging approach for interleaved power converters has been introduced. This approach combines both a wafer level packaging and a module level assembly. The fabrication and partial packaging at wafer level for vertical power diodes have been characterized from -50°C to +175°C without showing any abnormalities. The result is a true compact 3D assembly with outstanding electromagnetic interference and thermal characteristics.

#### Related Publications:

[1] N. Rouger, J. Widiez, L. Benaissa, B. Imbert, P. Gondcharton, B. Letowski, JC. Crébier, "3D packaging for vertical power devices", CIPS 2014, Feb. 2014, Numberg, Germany.

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by Layer Transfer Engineering: Application to 3D Packaging for vertical power devices", *IMAPS*, Tours, France, 2014.
[3] L. Di Cioccio, Y. Beillard, S. Mermoz, R. Estevez, P. Coudrain, S. Moreau, J. Widiez "Low temperature metal bonding for 3D and power device packaging", 4th IEEE International Workshop on Low Temperature Bonding for 3D Integration (LTB-3D), Tokyo, 2014. Invited paper.



# **High Efficiency Multijunction Solar Cells** for Concentrated PhotoVoltaics

## Research topics: CPV, Advanced Substrates

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#### Partnership: SOITEC, InPact, Fraunhofer-ISE Sponsorship: ADEME-Guepard

Current industry standard CPV cells are three-junction (3J) cells consisting in GaInP and GaInAs layers monolithically grown onto a Ge substrate by means of epitaxy. These structures had reached efficiencies up to 41,6% under concentrated sunlight illumination. Advanced 3J technologies even led to a 44,4% efficiency at 302 suns, but the performance can be further improved by adding additional junctions. Among the different potential technologies, wafer bonding is the most versatile one, allowing combination of non lattice matched III-V compounds. Here we present the record result of a bonded 4J cell and a path for cost effectiveness.

In this work, two separate growth runs led to an inverted GaInP/GaAs top tandem cell on GaAs and an upright GaInAsP/GaInAs bottom tandem cell on InP [1]. Excellent material quality was reached for all junctions, as they were grown lattice matched to the underlying substrate. Both wafers were chemical-mechanical polished to reach a root mean square surface roughness below 0.3nm as measured by atomic force microscopy. Wafer bonding process was optimized [2] to achieve a high bonding energy, a low electrical interface resistance and a high optical transmittance. Following bonding, the GaAs substrate was removed, leading to a GaInP/GaAs//GaInAsP/GaInAs fourjunction solar cell (see Fig.1). This combination is close to the ideal bandgap combination for a 4J device.

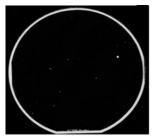




Figure 1: Left: Scanning acoustic microscopy image of a 100mm 4J solar cell wafer after bonding. Right: SEM cross section of the stacked

Front side and back side contacts were prepared at Fraunhofer ISE. IV-characteristics were measured using a spectrally adjustable solar simulator. Two consecutive world record efficiencies of 44.7% at 297 then further 46% at 508times concentration [5] of the AM1.5d (ASTM G173-03) spectrum were obtained (see Fig.2).

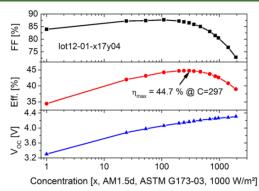


Figure 2: Summary of IV characteristics under concentration for the best four-junction GaInP/GaAs//GaInAsP/GaInAs solar cell. The efficiency maximum of 44.7% is reached at 297 suns. measurements were performed by the Fraunhofer ISE CalLab at temperature of 25°C.

In parallel the Smart-Cut™ technology applied to InP layer transfer has been extensively developed [3,4]. The Smart-Cut<sup>™</sup> technology can provide engineered substrates consisting on thin InP layer reported onto a host substrate, with advanced functions compared to the bulk InP substrates, especially in the field of optical efficiency, mechanical robustness or cost effectiveness. Moreover it offers the opportunity to re-use the same bulk InP wafers for multiple layer transfer, limiting both the cost and the consumption of InP raw material. We have experimentally demonstrated up to 5 full Smart Cut™ cycles and subsequent InP wafer refresh cycles, with no degradation of the transferred InP film defectivity.



Figure 3: (Left) 100mm wafer with thin InP transferred film on a new support substrate (sapphire in this case) following Smart-Cut<sup>TI</sup> technology. (Right) remaining InP wafer ready for recycling.

Combination of wafer-bonded 4J architecture with Smart- $\mathsf{Cut}^{\scriptscriptstyle\mathsf{TM}}$  technology for InP bulk wafers will enable cost competitive high efficiency CPV cells in the future.

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# Flexible Composites of Thermal Shape Memory Alloys and Piezoelectric Organic Materials

#### Research topics: Energy Harvesting, Functional Materials, Composites

B. Viala, B. Gusarov (G2ELab), S. Boisseau

#### Partnership: G2ELab

Energy harvesting (EH) is now considered as an alternative to battery-powered solutions. Recently a new class of harvesters based on smart materials or composites combining crossed-physical effects have been reported [1]. They open today novel hybrid-EH engineering for consumer products which is expected to play an important role to bridge the gap with conventional solid-state materials such as thermoelectricity (Seebeck effect) or pyroelectricity. When considering thermal sources which are the most prevalent in our environment, small spatial and time dependent temperature gradients are usually disregarded because it requires complex cold source management systems. The cold source usually consists in a radiator whose size and shape can be hardly optimized. Moreover, when wearable and flexible devices are targeted, solid-state materials combined with radiators can become a major constraint. We propose another scheme to get thin flexible thermal harvesters (TEH). The idea is to indirectly convert heat into electricity through mechanical transformations with thermal shape memory alloy (SMA) coupled to a piezoelectric material. In Fig.1, a thin flexible TEH composite is shown based on laminations of SMA and organic piezoelectric PVDF layers. This hybrid structure can generate voltage from temperature variations using two different energy conversion principles at once: pyroelectric and piezoelectric effects driven by SMA. So far only ceramic PZTbased composites have been experimentally demonstrated [1]. It may not however be an optimal choice, since even the flexible MFC piezoelectric composite from Smart Materials is limited to 0.45 % strain, whereas SMA can develop strain up to 3 %. In this work, PVDF is used as it withstands much larger strains and flexibility than ceramics and composites [2].

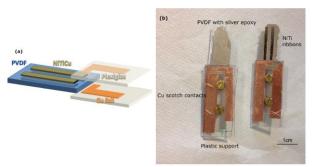


Figure 1: Schematic and optical images of the TEH laminated composite and PVDF alone, respectively.

Fig.2 shows the produced voltage of the composite with SMA effect which is 75% higher than the single pyroelectric output of PVDF. The corresponding energy is increased by

200 %. Finally, the energy density is 0.38mJ/cm³ which is much higher than that of the previous composite using MFC (0.095mJ/cm³).

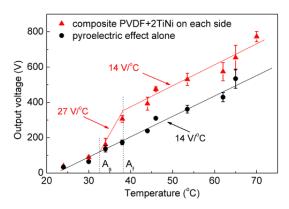


Figure 2: Experimental temperature dependence of output voltage for TEH laminated composite and PVDF alone, respectively.

To conclude, a novel flexible and thin composite thermal energy harvester is reported, which combines pyroelectric, piezoelectric and shape memory effect. The harvester combines superior flexibility of PVDF with large temperature-induced strain of the shape memory alloy (SMA) to harvest small and quasi-static temperature variations. The energy density is  $0.38 \, \text{mJ/cm}^3$  for a temperature change of  $20 \, ^{\circ}\text{C}$  in volume of  $30 \, \text{mm}^3$ . The harvester can successfully power a light-emitting diode (LED) instantaneously without any storage unit, see Fig.3. The use of PVDF quadruples the energy output, compared to previously reported PZT-based composites.

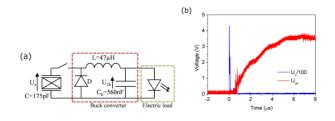


Figure 3: Circuit schematic and electric response of the Led-powered flexible hybrid TEH (raw harvested voltage in blue and voltage after conversion in red).

Related Publications:

[1] D. Zakharov, B. Viala, "Beyond CMOS Nanodevices Vol. 1 - Thermal Energy Harvesting Chap. 7", pp. 192-204, Francis Balestra (Editor), Wiley-ISTE, May 2014.

[2] B. Gusarov, D. Zakharov, E. Gusarova, B. Viala, O. Cugat, J. Delamare, L. Gimeno, "Thermal energy harvesting by combined pyroelectric, piezoelectric and shape memory effects", Sensors, Energy Harvesting, Wireless Network and Smart Objects (SENSO 2014), Oct. 22-24, 2014, Gardanne, France.



# Advanced Electrode Materials for Microbatteries

#### Research topics: Energy, Microbatteries

F. Le Cras, H. Porthault, S. Martin, R. Salot

## Partnership: STMicroelectronics, ICMCB, IPREM, ICMMO Sponsorship: PIA-TOURS2015

Electrode materials condition the main practical characteristics of lithium microbatteries that are their nominal voltage and nominal capacity, as well as their operation kinetics (i.e. current rates). These features are dependent on the redox couples involved along the lithium insertion/deinsertion process, the composition, the crystal structure, the electronic and ionic conductivities and the microstructure of the material, and also on the electrode/electrolyte interface properties.

Among positive electrode materials, LiCoO<sub>2</sub> is looked on as an ideal material; hence, it has been widely used in conventional Li-ion battery for more than 20 years. Indeed, its layered structure combined with the semiconductor to metal transition occurring in the early stages of the lithium deinsertion allow facile lithium and electron transports, and the involvement of the  $Co_4+/Co_3+$  couple leads to a high nominal voltage (4.2 V/Li+/Li). The main interests in using LiCoO<sub>2</sub> thin film electrodes is to build microbatteries able to supply the same voltage as the main power supply used in portable electronics (i.e. a Li-ion battery), and/or able to deliver high surface capacities, its superior transports properties allowing to use thicker electrodes. Crystallization of LiCoO<sub>2</sub> films deposited by sputtering requires a postannealing at high temperature (~700°C) which is not compatible with the underlying substrate. Thus, a complete study of the sputtering process was performed in order to enhance the ordering in the as-prepared film and to thermal budget for getting electrochemically active R-3m phase. Finally, a bias-assisted deposition process allowed to decrease the crystallization temperature to 500°C [1,2]. Nevertheless the deposition rate for the LiCoO2 film, which directly influences the cost of the whole microbattery, is still a real issue especially when a high film thickness is required. So, alternative deposition processes where also investigated, including sol-gel and hydrothermal routes. An innovative process combining electrodeposition and hydrothermal conditions has been identified and is under development (Fig.1). Present optimized process conditions allow a high rate deposition of LiCoO<sub>2</sub> on metallized Si wafers, i.e. 500 nm.min-1, and the achievement of thick electrode films [3]. Parallel to the optimization of deposition processes, the understanding of the electrochemical phenomena involved in the complete Li/LiPON/LiCoO<sub>2</sub> cell and further identification manufacturing defects and ageing phenomena are crucial to assess and to enhance the quality of the industrial process (EFL700 by STMicroelectronics). a dedicated fast characterization tool by Therefore. Electrochemical Impedance Spectroscopy (EIS) is currently developed [4].

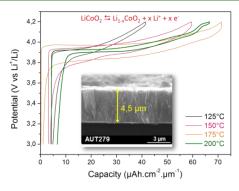


Figure 1: Voltage profiles of LiCoO2 thin films electro-deposited in hydrothermal conditions at various temperatures. Inset: Cross section of a LiCoO2 film deposited on a titanium plated Si wafer.

Alternative electrode materials to LiCoO2, providing much higher volumetric capacities and lower operating voltage, much suitable for energy harvesting devices and lowconsumption components, are developed for the next generations of microbatteries. Contrary to intercalation reactions (as in LiCoO<sub>2</sub>) which involve a limited amount of lithium due to the limited number of crystallographic sites, conversion reactions lead to the insertion a far larger amount of lithium per formula unit. Among promising materials, FeS2 (pyrite) [5] and CuO [6] were synthesized by sputtering and studied at first. The electrochemical behavior of FeS2 is quite interesting as it exhibits a very stable capacity, 5 times higher than LiCoO<sub>2</sub> (Fig.2). By the way, other candidate materials are also identified and yet under study.

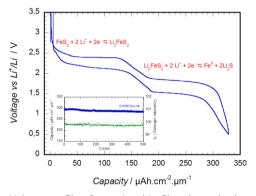


Figure 2: Voltage profile of a pyrite thin film electrode deposited by sputtering, then embedded in an all-solid-state Li/LiPON/FeS2 microbattery. Inset: Volumetric capacity retention over 500 cycles.

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  [6] L. Martin, H. Martinez, D. Poinot, B. Pecquenard, F. Le Cras, "Direct observation of important morphology and composition changes at the surface of the CuO conversion material in lithium batteries", *J. Power Sources*, 248, pp. 861-873, 2014.







Ab Initio Simulation for Advanced Devices

Quantum Simulation of FDSOI and Non-Planar Devices

Resistive RRAM: from Modeling to Simulation

Compact Modeling of Silicon Photonics Devices and
Their Integration in Standard EDA Tools



## **Ab Initio Simulation for Advanced Devices**

#### Research topics: RRAM, High-K, Graphene

P. Blaise, B. Traore, E. Vianello, G. Molas, C. Guedj, O. Renault, N. Barrett

Partnership: STMicroelectronics, U. Stanford, U. Campinas, CNRS-Néel, CEA-IRAMIS Sponsorship: Nanosciences Foundation

#### OxRRAM made with HfO<sub>2</sub> [1]

We have shown through experiments and ab initio simulations that the conductive state in nonpolar Pt/HfO<sub>2</sub>/Pt RRAM cells can be explained by local suboxide HfOx filaments, where x is close to or below 1.5 (Fig.1, left). The initial electroforming step not only promotes charge injection, but also stabilizes neutral O Frenkel pairs against charged O Frenkel pairs. This is important for filament formation that results from the accumulation of neutral O vacancy clusters. As the flow of electric current increases, temperature leads to O vacancy-interstitial recombination, and thus RESETs the device. The OFF-state resistance may further increase by thermal heating, indicating that there are O interstitials available near the suboxide filaments to recombine with O vacancies present in the filaments, (see Fig.1, right).

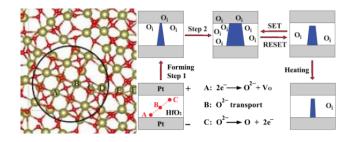


Figure 1: (left) Embedded Hf2O3 filament; (right) Schematic representation of the switching mechanism (blue regions are HfOx with x <= 1.5).

#### VEELS spectroscopy of HfO<sub>2</sub> [2]

We have measured VEELS spectra of pure m-HfO2 in correspondence to well-defined momentum transfer crystallographic directions. We have compared the experimental spectra to TDDFT calculated, finding a good agreement; (Fig.2). This has allowed us to correctly interpret and understand the dielectric properties of polycrystalline or monocrystalline m-HfO2 samples. We have found a significant anisotropy in the dielectric properties, mostly on the bulk plasmon at  $\sim\!16$  eV and on the dielectric constant.

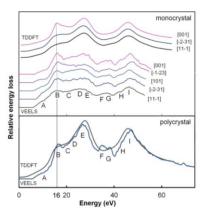


Figure 2: VEELS spectra measured and calculated with TDDFT (up panel: various crystallographic directions of monocrystal; down panel: average of polycrystalline sample.

#### XPEEM of graphene on SiC(0001) [3]

We have used high-resolution energy-filtered XPEEM and DFT calculations of a relaxed interface model to determine the work function (WF) of few layers graphene (FLG) on SiC(0001). WF values obtained from theory and experiments are found to be in qualitative agreement with an increase of the WF with each additional graphene layer, (Table 1). Compared to isolated graphene, the WF is modulated by the charge transfer from interface states to graphene, creating an interface dipole moment. In the calculations, the charge transferred is independent of the number of graphene planes, and this is consistent with the constant C 1s-SiC core-level binding energy measured by XPEEM. A layer dependent partial spill-out of the transferred charge is predicted theoretically, and explains the experimental C 1s-graphene core-level binding energy variations.

	SiC slab	SiC/BL	SiC/BL/1LG	SiC/BL/2LG	SiC/BL/3LG	SiC/BL/4LG
WF <sub>n</sub> (eV), calculated	3.60	3.65	4.31	4.55	4.75	4.76
$WF_n$ (eV), measured	_	_	$4.28 \pm 0.03$	$4.34 \pm 0.03$	$4.39 \pm 0.03$	_
C 1s BE (eV)	283.7		$284.57 \pm 0.05$	$284.48 \pm 0.05$	$284.40 \pm 0.05$	
Interface dipole (eV)	_	_	1.14 (20.35)	1.41 (26.25)	1.64 (48.41)	1.64 (114.22)
Charge transferred (e Å <sup>-2</sup> )	_	_	0.0026 (0.011)	0.0029 (0.010)	0.0030 (0.008)	0.0030 (0.007)
Charge spill-out (%)	_	_	16.1	10.3	9.7	8.4

Table 1: Calculated and measured WFs, measured core-level binding energies, calculated interface dipoles, calculated charge transferred from SiC to FLG, and calculated charge spill-out.

#### Related Publications:

[1] K.H. Xue, B. Traore, P. Blaise, L.R.C Fonseca, E. Vianello, G. Molas, B. de Salvo, G. Ghibaudo, B. Magyari-Kope, Y. Nishi, "A Combined Ab Initio and Experimental Study on the Nature of Conductive Filaments in Pt/HfO2/Pt Resistive Random Access Memory", *IEEE Transactions on Electron Devices*, Vol. 61, 1394, 2014.

Transactions on Electron Devices, Vol. 61, 1394, 2014.
[2] C. Guedj, L. Hund, A. Zobelli, P. Blaise, F. Sottile, V. Olevano, "Evidence for anisotropic dielectric properties of monoclinic hafnia using valence electron energy-loss spectroscopy in a high-resolution TEM and ab initio time-dependent density-functional theory ", Appl. Phys. Lett., 105, 2014.

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# **Quantum Simulation of FDSOI and Non-Planar Devices**

#### Research topics: FDSOI, Tri-gate, Nanowire, Quantum Simulation

F. Triozon, Y.-M. Niquet, V.-H. Nguyen, I. Duchemin, J. Li, D. Rideau (STM), O. Nier (STM), S. Guarnay, S. Martinie, A. Bournel (IEF)

# Partnership: CEA-INAC, STMicroelectronics, IEF Orsay Sponsorship: ANR-NOODLES

CEA-INAC and CEA-Leti have developed a 3D quantum transport solver based on the Non-Equilibrium Green's Functions (NEGF) method [1]. It allows the simulation of realistic device geometries with interface roughness and random distributions of charged impurities. In 2013, the ability of this solver to address the silicon devices fabricated at CEA-Leti and STMicroelectronics was demonstrated. In 2014, the NEGF solver has been extensively used to study carrier mobility in FDSOI devices. A very good agreement with experiments has been shown for planar devices [2,3]. Then the NEGF solver has been successfully applied to the tri-gate silicon devices fabricated at CEA-Leti [3]. Besides this, the performances of short channel FDSOI devices in the quasi-ballistic regime have been investigated by means of Monte Carlo simulations [4].

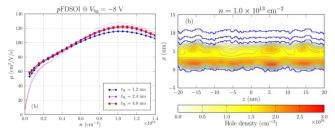


Figure 1: Left: Hole mobility vs. density in a planar UTBB-FDSOI device at room temperature and back-gate voltage Vbg = -8 V, for various interfacial layer thicknesses (solid lines: NEGF simulation, dotted lines: experiment). Right: hole density map from the NEGF simulation.

FDSOI devices with ultra-thin body and BOX (UTBB) feature back-gate electrostatic control, which allows tuning the threshold voltage and can also increase the carrier mobility in the ON state. The mobilities computed with NEGF (see methodology in [1]) have been calibrated on the extensive experimental database available at STMicroelectronics. This validation task on planar devices was mandatory before applying the NEGF solver to non-planar architectures. The calibration, which consists in the adjustment of the scattering parameters, was successful. Both electron and hole experimental mobilities were reproduced using the same structural parameters (material thicknesses, interface roughness amplitudes, and density of remote charges in the gate stack). Moreover, without changing any parameter,

simulations matched a large set of experimental data with different interfacial oxide layer (IL) thicknesses, different temperatures, and different back-gate and front-gate voltages [2,3]. A typical NEGF simulation of hole mobility is shown in Fig.1, together with the experimental mobility, at back-gate voltage Vbg = -8 V. In this back channel inversion regime, the IL thickness has a weak impact on the mobility.

The NEGF solver shows its full potential for non-planar architectures, in which quantum confinement plays a prominent role. We have simulated the mobility of the trigate silicon transistors fabricated at CEA-Leti. Again, keeping the same structural parameters for NMOS and PMOS, the experimental electron and hole mobilities were well reproduced at different temperatures [3]. Fig.2 shows the simulation of hole mobility at room temperature.

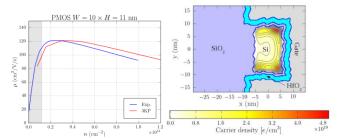


Figure 2: Left: Hole mobility vs. density in a tri-gate silicon transistor at room temperature (red line: 3D NEGF simulation, blue line: experiment). Right: hole density map from the NEGF simulation.

All these calibration studies only addressed the long channel low field mobility. The next step is the simulation of the next generations of ultra-short channel devices in their target operating voltages. The importance of contact and ballistic resistances in short channels has been evaluated by Monte Carlo simulations [4]. Recent developments of the NEGF solver allow a realistic description of the access regions (discrete dopants distributions) and the inclusion of non-uniform strain fields. This offers promising perspectives for the simulation and optimization of future CMOS technologies.

The NEGF simulations were performed on the TGCC/Curie machine using PRACE and GENCI allocations.

<sup>[1]</sup> Y.-M. Niquet et al., "Quantum calculations of the carrier mobility: Methodology, Matthiessen's rule, and comparison with semi-classical approaches", Journal of Applied Physics 115, 054512, 2014.

<sup>[2]</sup> V.-H. Nguyen et al., "Quantum modeling of the carrier mobility in FDSOI devices", IEEE Transactions on Electron Devices, Vol. 61, 3096, 2014.

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International Workshop on Computational Electronics (IWCE 2014), June 3-6, 2014, Paris, France, invited talk.
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# **Resistive RRAM: from Modeling to Simulation**

# Research topics: CBRAM, OxRRAM, TCAD Simulation, Compact Modeling

O. Cueto, M. Reyboz, P. Dorion, A.Payet, F. Longnos, T. Benoist, N. Jovanovic, E. Vianello, G. Molas

#### **Partnership: ALTIS Semiconductor**

In the Simulation and Modeling Laboratory, in-house TCAD simulation tool and compact model dedicated to Oxide Resistive Memory (OxRRAM) and Conductive Bridging Random Access Memory (CBRAM) are being developed. The main target is to support technological developments and the design of innovative circuits using OxRRAM and CBRAM cells.

#### TCAD Simulation

An electro-thermal resistive switching model based on O-Frenkel pairs has been developed [1] to simulate reset and set mechanisms for HfO<sub>2</sub>-based OxRRAM devices. It relies on a filamentary conduction mechanism based on the breaking of Hf-O bonds, generation of O-Frenkel pairs  $(V_0^{2+}/O_i^{2-}),$  migration of  $O_i^{2-}$  under high electric field and elevated temperature. Breaking of conductive filament is modeled by recombination of  $V_0^{2+}/O_i^{2-}$  as illustrated by Fig.1.

Simulated devices are 1T/1R HfO<sub>2</sub>-based RRAM cells relying on 65nm CMOS technology

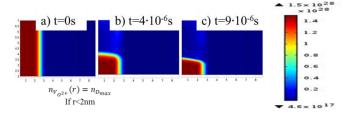


Figure 1: Evolution of  $n_{V_0^{2+}}$  during reset simulation.

Broadly accepted physical mechanism involved in CBRAM is a resistance switching induced by electro-chemical driven growth and rupture of a metallic-like filament in an electrolyte. Our TCAD simulation tool based on the finite element discretization of a system of partial differential equations coupled to the Level Set method [2]. has been extended to take into account the presence of Ag-rich clusters in GeS2 electrolytes as illustrated by Fig.2.

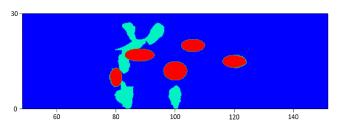


Figure 2: Ag filament (in blue) growth with Ag-rich clusters (in red).

#### Compact model

To design innovative circuits using CBRAM, a compact model is mandatory. This model should be fast, robust and accurate. We proposed a continuous physical compact model, written in Verilog-A valid for chalcogenide and metal-oxide based CBRAM.

Main characteristics of CBRAM cells are simulated with the developed model and calibrated on electrical measurements as the set and reset switching time on Fig.3.

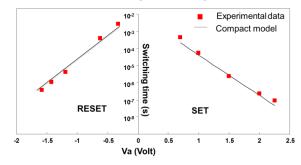


Figure 3: comparison between measurements and model of the switching time versus applied voltage for SET and RESET.

Moreover, variability is a crucial issue for this kind of memory. Thus, we define the typical case (TT) and four corners which represent extreme values of the low (L) and high (H) resistances, Fig.4, for the typical programming condition [4]. In order to design robust circuits, the worst case (HL) should be chosen and to design innovative circuits, designers should use the best case (LH).

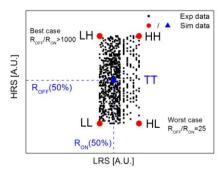


Figure 4: corner plot of the Low (LRS) and High (HRS) Resistive States.

The model is incorporated in Cadence design flow using Eldo simulator allowing design of innovative circuits. Different electrical circuits are tested to prove the robustness of the proposed model.

#### Related Publications:

[1] O. Cueto et al., "Development of an electro-thermal resistive switching model based on O-Frenkel pairs to study reset and set mechanisms in HfO2-based RRAM cells", 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2014), Sept. 9-11, 2014, Yokohama, Japan.

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# Compact Modeling of Silicon Photonics Devices and Their Integration in Standard EDA Tools

#### Research topics: Photonics, Compact Modeling, Process Design Kit

P. Martin, F. Gays

Partnership: Mentor Graphics Sponsorship: IRT Nanoelec.

Fabrication of Application Specific Photonics Integrated Circuits (ASPICs) will bring substantial breakthroughs in very high speed data communications, telecommunications and supercomputing. Among other photonics integration technologies, silicon photonics is probably one of the most serious industrial candidates due to its potential large-scale and low-cost production capability in existing CMOS foundries. To duplicate the success story of integrated circuits to ASPICs, the industry must fully adapt the technology platform to address photonics-specific requirements. One of the key challenges at the design level is to develop an Electronic Design Automation (EDA) flow fully compatible with standard CMOS methodology and tools. Efficient CAD tools are required all along the design process, in particular during modeling of silicon photonics devices and circuits.

Models developed in the Verilog-A behavioral language have the advantage of allowing the devices to be used in commercial SPICE circuit simulators. However there are relatively few publications on modeling of photonics devices using Verilog-A and their incorporation in a standard design environment.

Here, we present a new modeling approach and the introduction of models of photonics devices in standard EDA tools [1-2].

Up to now, only optical power (in Watt) and phase (in radian) were considered. However, in some optical devices light is polarized and passive optical devices are bidirectional (light coming from left to right or from right to left). So, we introduced a new concept: an optical signal composed of 9 different lines (Fig.1) which are grouped in an optical bus by analogy with an electrical bus such as the IEEE-488 bus.

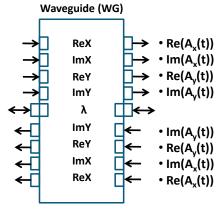


Figure 1: The 9 lines of the optical bus for a waveguide. Ax and Ay are the complex amplitudes of the two polarization modes and  $\lambda$  the central wavelength during simulation.

We developed a toolbox for Silicon on Insulator (SOI) photonics (Fig.2). The following Verilog-A models are available for passive and active devices: silicon waveguide, grating coupler, MMI 1x2 and 2x1 couplers, MMI 2x2 coupler, cross coupler, Ge PIN photodiode, Mach-Zehnder modulator with heater, laser optical source, optical termination, etc. Impact of the SOI technology is considered by taking into account the influence of interconnections, coupling capacitances and high resistivity of the silicon wafer at high frequency.

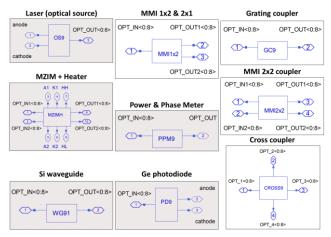


Figure 2: SPICE toolbox of passive/active silicon photonics devices and symbols.

The photonics ASPICs design flow is presented in Fig.3.

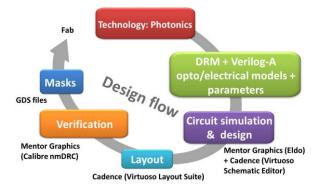


Figure 3: Photonics PDK and ASPICs design flow.

#### Related Publications:

[1] P. Martin, F. Gays, E. Grellier, S. Menezo, "Development of Verilog-A models for silicon photonics devices and implementation in a standard EDA environment", *MOS-AK Compact Modeling Workshop*, London Metropolitan University, March 28-29, 2014.
[2] P. Martin, F. Gays, E. Grellier, A. Myko, S. Menezo, "Modeling of Silicon Photonics Devices with Verilog-A", *Proceedings of the 29th Int. Conf. on Microelectronics*, pp. 209-212, Belgrade, Serbia, 12-15 May 2014.







Silicon Interposer Technology for 2.5D and 3D Integrated RF/mmW Systems

Sol-Gel Ferroelectric Thin Films for RF Tunable Capacitors

Thin Monocrystalline Piezoelectric Films for Acoustic Resonators, Filters and Sensors

Spin Torque Oscillators for Telecom Applications



# Silicon Interposer Technology for 2.5D and 3D Integrated RF/mmw Systems

#### Research topics: Si Interposer, Integrated Antennas, Metamaterials

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Partnership: DGA Sponsorship: CARNOT Funding

The interest in millimeter-wave (mmw) frequency bands has been constantly rising across the last decade. New applications such as sub-THz imaging and automotive radar are shaping the future of the next generation of smart devices. As for communication systems, higher data rates in the range of a few Gbps at short-range are nowadays achievable thanks to a larger RF bandwidth (up to 9 GHz for the 60 GHz ISM band). This progress has benefited from the advances in silicon-based RFIC front-end design; mostly inherited from CMOS technology which was initially dedicated to digital and low frequency analog applications. However, the antenna stage's footprint is still an issue due to the fundamental relation between the radiator's effective area and the achievable gain. However, it is known that CMOS integrated antennas-on-chip (AoC) suffer from low radiation efficiency (below 20 %).

Antenna-in-Package (AiP) approach using silicon interposer seems to be a good candidate to solve this issue: vertical stacking offers compact 3D integration capabilities as well as very good thermal dissipation properties. Moreover, using high-resistivity silicon substrates ( $\rho>1 k\Omega.cm$ ), radiation efficiencies in the range of 50 % could be targeted [1].



Figure 1: Novel HIS designs enabling cavity-less integration.

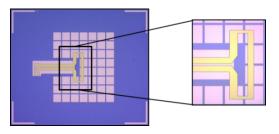


Figure 2: Microphotograph of the integrated 60GHz antenna with HIS reflector.

We have investigated a new mmw packaging approach based on silicon interposer with a new type of integrated and efficient antennas. The aim of this approach is to mimic an artificial magnetic conductor's (AMC) behavior with a near-zero reflection (at least in the frequency band of interest) allowing the reflector to be placed in the vicinity of the radiating element (from 10  $\mu m$  to 20  $\mu m$  at 60 GHz).

The resulting patterned structure is called High-Impedance Surface (HIS). This new structure allows moving towards

"real 3D" integration, where the RFIC could be eventually placed directly below the antenna and fed using Through-Silicon Vias (TSV) as illustrated in Fig.1.

The 200 µm-thick interposer has been designed and microfabricated in CEA-Leti's 200 mm facilities. Fig.2 illustrates one of the implemented designs with an overall area of 3x2.5 mm² as referred to in [2]. These integrated antennas have been fully characterized in anechoic chamber over multiple frequency points as shown in Fig.3. The realized gain in reported for different frequency points in the Fig.4. A 5 dBi gain is achieved with excellent cross polarization isolation

(-25 dB) and bandwidth (10 % using -10 dB). The achieved radiation efficiency extracted from measurement data is higher than 40% over the band of interest for HR silicon prototypes.

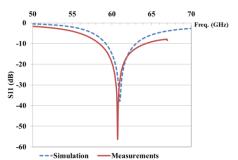


Figure 3: Reflection coefficient of a single antenna.

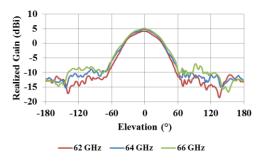


Figure 4: Realized gain of the two-element antenna array in H-Plane.

This illustrates the strong potential of silicon in an AiP approach, and paves the way to compact and smart millimeter-wave interposers in the future for demanding applications such as LTE, 5G telecommunications and THz imaging.

Related Publications:

[1] O. El Bouayadi, Y. Lamy, L. Dussopt, "A High-Impedance Surface Antenna On Silicon Interposer for 3D Integrated mmW Transceivers", European Microwave Conference (EuMC), Rome, Italy, Oct. 5-10, 2014.

[2] O. El Bouayadi, Y. Lamy, L. Dussopt and B. Soulier, "A New Approach for Reliable and Compact 3D Integration of mmW Transceivers on Silicon Using High-Impedance Surface Antennas", 47<sup>th</sup> International Symposium on Microelectronics (IMAPS 2014), San Diego, USA, Oct. 14-16, 2014.



# Sol-Gel Ferroelectric Thin Films for RF Tunable Capacitors

#### Research topics: Integrated RF Capacitors, High Tunability, Sol-Gel Ferroelectrics

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Partnership: STMicroelectronics Sponsorship: PIA-Tours2015

As digital systems move toward higher frequencies and high data rates, it becomes extremely challenging to supply novel low-cost and highly efficient integrated passives to gradually replace discrete components. Voltage-tunable capacitors are essential components in many radio-frequency applications such as voltage-controlled oscillators adaptive impedance matching circuits. Semiconductor varactors, generally used in RF circuits, can provide considerable capacitance tuning. However, they usually suffer from a large series resistance that increases with increasing capacitance tuning. Thus, it is fundamentally impossible to obtain a large tunability combined with a high quality factor (Q). Recently, ferroelectric thin films have particularly attracted considerable interest for voltage tunable applications since they offer a host of advantages over varactor diodes. These include low cost simultaneous fabrication of multiple parts, large dielectric nonlinearity under dc bias field, low losses, and minimal frequency dispersion.

Lead zirconate titanate (PZT) which is actively investigated and used in a many industrial domains including non-volatile memories, micro-electro-mechanical systems (MEMS), is especially well-known candidate materials for tunable capacitor applications due to their remarkable ferroelectric properties and stability in device operating ranges. However, in order to achieve a viable replacement for varactor diodes, there are several issues that PZT-based capacitor must address. At first, reported voltage tunability of PZT films in the high frequency range is relatively low (~35%) and remains insufficient for microwave tunable devices. performance Therefore. optimization needs to accomplished by improved material processing compositional adjustment. To this end, much attention has been focused on the modification of PZT by adding a small amount of dopants. Secondly, the development of low-cost procedures to prepare PZT-based thin films is an inevitable step towards meeting the requirements of today's microelectronics industry.

Here, manganese (Mn)-doped PZT (PMZT) RF capacitors have been developed using a sol-gel process [1]. Indeed, the sol-gel deposition route is of significant interest for thin film capacitors applications from an industrial point of view. It provides a good compatibility to photolithography and allows low temperature processing, large area coating ability, precise composition control and cost reduction. Metalinsulator-metal (MIM) capacitors using sol-gel PMZT have been successfully processed on platinized 200 mm silicon wafers (Fig.1). On-wafer electrical analyses have been conducted with a particular attention to leakage current characterization and radiofrequency measurements under DC bias voltage. For this, an accurate and reproducible characterization methodology has been set up beforehand by

investigating influence of experimental conditions such as atmosphere on electrical measurements [2]. Dielectric properties of PMZT thin films have then been compared to those of conventional PZT layers.

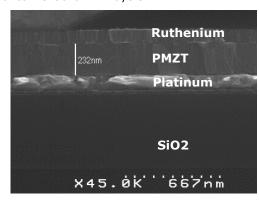


Figure 1: SEM cross-section of the sol-gel PMZT thin film capacitors.

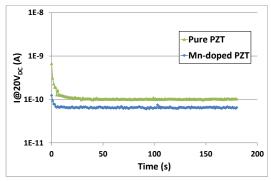


Figure 2: Leakage current of pure PZT and PMZT at 20V<sub>DC</sub>.

The dielectric response analysis of PMZT thin films revealed an enhanced tunability achieving 85% ( $\sim$ 7:1) at 1 GHz. Besides, the leakage current density decreased from 6.5  $\mu$ A/cm² to 1  $\mu$ A/cm² at 850kV/cm by doping PZT with Mn (Fig.2). Thus, PMZT tunability is among the highest ones reported in the literature for PZT-derived thin films but also for other piezoelectric materials. Indeed, in comparison, the tunability of BST-based materials, typically studied for voltage tunable applications, does not exceed 5:1. These remarkable results indicate that Mn-doped PZT thin films are promising candidates for RF tunable capacitors..

<sup>[1]</sup> W. Benhadjala, F. Sonnerat, J. Guillaume, C. Dieppedale, P. Renaux, M. Bousquet, G. Le Rhun, H. Sibuet, C. Billard, "Electrical characterization of Mn-doped PZT thin films for integrated microwave devices", *Piezoelectric Micro and Nano Structures and their Applications Conference*, Sept. 25-26, 2014, Blois, France.

<sup>[2]</sup> W. Benhadjala, F. Sonnerat, J. Guillaume, P. Renaux, M. Bousquet, H. Sibuet, C. Billard, "On-wafer electrical characterization of piezoelectric thin films for RF tunable capacitors", *Piezoelectric Micro and Nano Structures and their Applications Conference*, Sept. 25-26 2014, Blois, France.



# Thin Monocrystalline Piezoelectric Films for Acoustic Resonators, Filters and Sensors

## Research topics: Thin Film Transfer, Quartz, Lithium Niobate, BAW Resonators

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#### Partnership: FEMTO-ST, ONERA, FrecNSys

The increasing complexity of RF front ends, driven by the multiplication of mobile phone frequency bands (more than 40 currently used in modern data hungry mobile phones), puts a strong pressure to develop new system architectures. In this context, the conventional Bulk Acoustic Wave (BAW) filters used to improve the linearity of the front end are facing considerable challenges and have to overcome limitations in terms of insertion loss, roll-off sharpness, temperature stability and rejection. This requires the capability to provide resonators with improved quality factors, electromechanical coupling factors, ideally with reduced temperature dependence. Making these filters frequency agile would even be a must.

Currently, conventional resonator performances rely on the piezoelectric properties of the materials they are made off, generally aluminum nitride (AIN). Replacing this material by piezoelectric thin films of lithium niobate (LiNbO<sub>3</sub>) would provide a dramatic increase in electromechanical coupling factor, which could be traded for improved quality factors, larger bandwidths, or for frequency agility.

LiNbO3 is however very difficult to grow with the necessary material quality, due to the difficulty to control the Li/Nb stoichiometry. Moreover, the natural growth orientation (caxis) is not the one exhibiting the best piezoelectric properties (a-axis). Therefore, we opted for an alternative approach, based on the transfer of LiNbO3 films, either through ion-slicing if sub-micrometer thick films are required, or wafer-bonding and thinning to reach thicknesses of several micrometers. The later technique was recently applied to transfer a 5 µm-thick X-cut LiNbO3 film onto a silicon wafer [1], as shown in Fig.1. W electrodes were inserted in the material stack before wafer bonding. BAW resonators were then fabricated by depositing and patterning Al electrodes, and eventually releasing the piezoelectric film through deep reactive ion etching of the silicon substrate. The electrical response shown in Fig.2 exhibits an electromechanical coupling factor of 53%, what is suitable for the implementation of filters with a tuning range of close to 15 %. Future works will aim at improving the quality factors of those resonators.

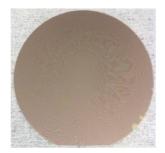


Figure 1: Photograph of a 5  $\mu$ m-thick LiNbO3 film transferred onto a 100 mm silicon substrate.

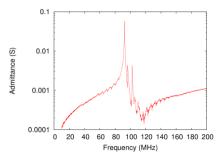


Figure 2: Electric response of a LiNbO3 BAW resonator.

Such an approach also benefits to sensor applications. For example, a quartz thin film has been transferred onto silicon substrates [2], for the purpose of fabricating piezoelectric These sensors take the form of tuning forks that are excited to vibrate into an in-plane vibration mode, and whose out of plane vibration mode is used to sense the mechanical accelerations. Fig.3 shows the process flow employed to fabricate these devices, including the transfer of the piezoelectric film onto pre-formed cavities, while Fig.4 shows the resulting tuning forks. Electrical measurements reveal resonances with quality factors close to 12,300 at 90 kHz under vacuum, close to the viscoelastic limit of quartz, showing that the single crystal material quality is maintained throughout the developed process. This opens interesting perspectives with respect to the integration of quartz resonators onto silicon.

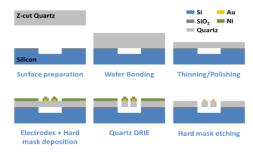


Figure 3: Process flow for the transfer of quartz onto pre-formed cavities and the fabrication of a quartz tuning fork.

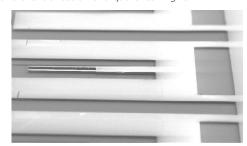


Figure 4: SEM photograph of a transferred quartz tuning fork.

#### Related Publications:

[1] A. Reinhardt, L. Benaissa, J.B. David, N. Lamard, V. Kovacova, N. Boudou, E. Defaÿ, "Acoustic filters based on thin single crystal LiNbO3 films: status and prospects", 2014 IEEE Ultrasonics Symposium, Sept. 3-6 2014, Chigago, USA.

[2] S. Grousset, P. Lavenus, L. Benaissa, R. Taïbi, E. Augendre, T. Signamarcheix, O. Le Traon, S. Ballandras, "Quartz-based vibrating MEMS fabricated using a wafer-bonding process with sealed cavities", 2014 International Frequency Control Symposium (IFCS2014), May 19-22, 2014, Taipei, Taiwan.



# **Spin Torque Oscillators for Telecom Applications**

# **Research topics: Spintronic, RF Components**

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#### Partnership: DSM-INAC-SPINTEC Sponsorship: ANR-SPINNOVA, FP7-MOSAIC

Spin Torque Nano-Oscillators (STNO) are nano-sized radio-frequency auto-oscillators whose frequency can be tuned in a wide range by variation of the bias direct current (DC) driving the STNO. The STNO frequency tuning originates from the nonlinear properties of the magnetization dynamics induced by spin transfer torque in a multilayered magnetic nanostructure. STNOs are of interest for the realization of integrated microwave components in which the modulation is used to code and process signals. The modulation is also important in the recently proposed STNO-based "dynamic read head" for data storage, where the modulation signal is provided by the stray magnetic field of a recorded bit. For such applications, it is important to understand whether an upper limit of the modulation bandwidth exists and, if so, what parameters drives it.

One of the most critical characteristics of spin torque nanooscillators (STNO) is the speed at which an STNO responds to variations of external control parameters, such as current or/and field. Theory predicts that this speed is limited by the amplitude relaxation rate  $\Gamma p$  that determines the timescale over which the amplitude fluctuations are damped out. This limit can be verified experimentally by analyzing the amplitude and frequency noise spectra of the output voltage signal when modulating an STNO by a microwave current [1]. Modulation is studied in the situation when both the bias DC current (to generate the oscillation) and an RF modulation current (to modulate the STNO-generated signal) are applied to an STNO simultaneously. This corresponds to a direct modulation of the generated microwave signal. It is illustrated in Fig.1 where the output voltage signal of a magnetic tunnel junction STNO with a stack composition PtMn/CoFe/Ru/CoFeB/MgO/CoFe/CoFeB is shown to oscillate in time in response to an RF current at the modulation frequency of fm=4MHz.

The amplitude and frequency noise spectroscopy technique based on the analysis of time traces of the STNO output voltage signal V(t), has been applied to STNOs based on both MTJ and spin-valves. This technique allows one to separate the noise signals from the modulated signal and confirms the general theoretical prediction for non-isochronous auto-oscillators that the amplitude relaxation rate  $\Gamma p$  is the central parameter that limits the speed of an STNO response to an external control signal. Such a limit is shown to play a crucial role not only in modulation, but also in the injection locking experiments, where the transient time from the "free running" to the "injection locked" states is limited by  $\Gamma p$  [2,3]. Furthermore the developed experimental method allows one to determine the amplitude relaxation rate of an auto-oscillator with relatively low output power such as spin valves (see Fig.2).

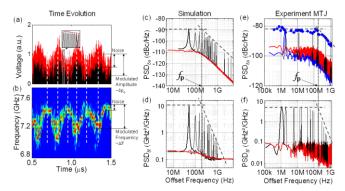


Figure 1: Time evolution of the STNO (a) output voltage and (b) frequency under rf current modulation. (c) to (f): Amplitude noise PSD from (c) simulation and (e) experiments and frequency noise PSD from (d) simulation and (f) experiments.

In Fig.1 (c) to (f), red lines are the noise PSD (amplitude and frequency) of the unmodulated signal. In (e) the blue line is the measured amplitude noise of the modulated signal. Superposed onto the unmodulated signal (red) are the peaks (black) appearing in the noise PSD of the modulated signal obtained at different modulation frequencies. The blue dotted points in (e) correspond to the peak power of the modulation peaks obtained from different experiments upon varying the modulation frequency fm. The envelope of these peaks (i.e. dashed lines) show a roll-off at fp (amplitude relaxation frequency).

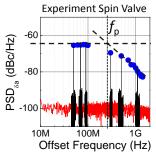


Figure 2: Amplitude noise PSDs for a 100nm spin valve STNO device modulation based on the following magnetic stack (in nm) PtMn(20)/  $Co_{80}Fe_{20}(2.5)/Ru(0.8)/[Co_{80}Fe_{20}(1)/Cu(0.3)]2/Co_{80}Fe_{20}(1)/Cu(3)/Co_{80}Fe_{20}(1)/Ni_{80}Fe_{20}(2)$  under rf current.

The value of the relaxation frequency, fp, as determined for the investigated mode is around one hundred MHz for currents close to the critical current. This is a limitation for applications that aim at GHz modulation rates in telecommunications or at Gbit/sec bit data rates in data storage applications. However numerical studies show that other STNO excitation modes can lead to values of fp in the GHz range.

#### Related Publications:

[1] M. Quinsat, F. Garcia-Sanchez, A. S. Jenkins, V. Tiberkevich, A. N. Slavin, L.D. Buda-Prejbeanu, A. Zeltser, J. A. Katine, B. Dieny, M.-C. Cyrille, U. Ebels "Modulation bandwidth of spin torque oscillators under current modulation", *Applied Physics Letters*, Vol.105, Issue 15, Oct. 2014.

[2] M. Tortarolo, C. Dieudonné, M. Quinsat, L. Buda-Prejbeanu, M-C. Cyrille, U. Ebels, "Phase noise analysis of a noisy spin torque oscillator synchronized to an external signal", 59<sup>th</sup> Magnetism and Magnetic Materials conference, Nov. 3-7, 2014, Honolulu, USA.

[3] C. Dieudonné, L. Buda-Prejbeanu, M. Zarudniev, M. Tortarolo, O. Klein, M-C. Cyrille, U. Ebels, "Coupling sensitivity of injection-locked spin torque oscillators at simple and double driving frequencies", 59<sup>th</sup> Magnetism and Magnetic Materials conference, Nov. 3-7, 2014, Hopping U.S.A.







# MEMS Actuators & Sensors & Reliability

Physical Origin of Piezoelectric Properties in PZT

New In-Line Measurement Techniques of PZT Piezoelectric Coefficients

**MEMS Actuators for Haptic Applications** 

Highly-Doped Suspended Silicon Nanowires for Gas Sensing by Thermal Conductivity Monitoring

Study on Linearity and Fatigue Resistance of Piezoresistive Nanogauges in M&NEMS Structures

Dual-Mode Probe for Ultrasonic Imaging and Therapy Based on cMUT Technology



# **Physical Origin of Piezoelectric Properties in PZT**

# Research topics: Piezoelectric Actuators, Thin Film Materials

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#### Sponsorship: DGA

Lead-based films like  $Pb(Zr,Ti)O_3$  (PZT) are known to exhibit piezoelectric properties, at morphotropic phase boundary (MPB). For PZT, the MPB corresponds to the Zr/Ti atomic ratio close to 52/48. Three phases coexist at this composition, namely tetragonal, rhombohedral and monoclinic. This phase coexistence and consequently the polarization mobility increase are thought to be the reason why piezoelectricity is enhanced in the MPB region. In 2011, Hinterstein *et al.* showed by in situ observations that bulk ceramic MPB PZT experiences a tetragonal-to-monoclinic phase transition while electric field is applied [1]. An open question is therefore whether there is a correlation between large piezoelectric effects and this field-induced phase transition. Today, it is widely believed that most of the piezoelectric effect is induced by domain wall switching.

In this paper, we show that MPB PZT films experience in situ structural modifications versus electric field. We aim to correlate this field-induced phase transition with PZT films piezoelectric properties. This correlation could have a strong impact on piezoelectric material design for applications, as inkjet devices, integrated optical lenses or micro-actuators in general.

PZT thin films at MPB were prepared by spin-on sol-gel method. Capacitors were realized by depositing 5 x 5 mm² squared top electrode. X-Ray diffraction (XRD) measurements were performed while applying a dc-electric field (Fig.1). The PZT XRD profiles were analyzed using two crystallographic space groups, namely tetragonal P4mm and rhombohedral R3m.

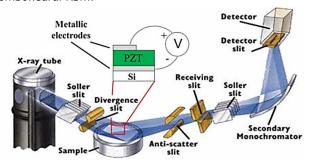


Figure 1: XRD setup for in-situ observation on PZT film capacitors.

Fig.2 shows the Bragg-Brentano diffraction profiles around (400) peaks at different voltages. This peak shifts towards lower angles when voltage is applied. The peak amplitude decreases with voltage. The amount of (004) P4mm phase, that is to say tetragonal c-domains, is invisible here and it does not change with voltage.

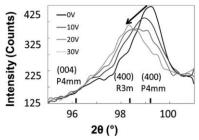


Figure 2:  $\theta$ -2 $\theta$  profile evolution of PZT around peak (400) vs voltages.

The relative volume proportion of phases P4mm and R3m versus voltage has been determined with MAUD software (Fig.3). Hence R3m stands for 40% of the phase volume at 0 V and 100% at 30 V. As P4mm and R3m are the only phases, the increase of R3m amount with voltage magnitude means that P4mm volume decreases accordingly, that is to say there is a voltage-induced phase transition. Besides, the fit gives the opportunity to roughly extract d33,eff. Indeed, we know (1) the amount of volume phase that has transited from P4mm to R3m (60% at 30 V) and (2) the peaks position (98.2° for R3m and 99.2° for P4mm). It gives d33,eff = 150 ± 25 pm/V at 30V, which is in the range of what has been measured with the DBLI method (120-130 pm/V) by AixACCT. Therefore, it proves that the piezoelectric effect of this MPB PZT film is mostly due to the voltageinduced transition from tetragonal to rhombohedral phases [2,3].

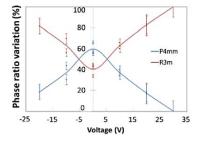


Figure 3: P4mm and R3m phase ratio variation versus electric field.

In this paper, we observed by in operando X-Ray diffraction that a tetragonal to rhombohedral phase transition is experienced by MPB 52/48 PZT thin films when an external electric field is applied. Besides, the film piezoelectric coefficient d33,eff measured on the one hand with a piezoelectric set-up and on the other hand deduced from X-Ray peak displacements versus the applied field appeared very similar. This proves that there is a strong correlation between the piezoelectric properties and the field-induced phase transition in MPB PZT films. This result suggests that one could probably improve even further d33,eff by favoring the field-induced phase transition notably by fine tuning PZT film composition.

- [1] Hinterstein *et al.*, "Structural Description of the Macroscopic Piezo- and Ferroelectric Properties of PZT", *Phys. Rev. Lett.* 107, 2011. [2] V. Kovacova *et al.*, "Correlation between electric-field-induced phase transition and piezoelectricity in lead zirconate titanate films ",
- Physical Review B 90, 140101(R), 2014. [3] V. Kovacova et al., "Enhancement of piezoelectric properties in Pb(Zr,Ti)O<sub>3</sub> thin films by electric field induced phase transition", Ultrasonics Symposium (IUS 2014), 3-6 Sept., 2014, Chicago, USA (poster).



# New In-Line Measurement Techniques of PZT Piezoelectric Coefficients

#### Research topics: Piezoelectric Actuators, Thin Film Materials

G. Le Rhun, F. Casset, T. Schmitz-Kempen (AixACCT), E. Defaÿ

# Partnership: AixACCT GmbH, Xaar Technology Ltd, IEMN-ISEN, MENAPIC, STMicroelectronics Sponsorship: KET-Lab4MEMS

Piezoelectricity is among the most suited functionality for electromechanical systems as strong electro-mechanical coupling can be reached. The piezoelectric effect is reversible in that materials exhibiting the direct piezoelectric effect (generation of electrical charges in response to applied mechanical stress) also show the converse piezoelectric effect (generation of mechanical strain as a response of an applied electric field), thus allowing to realize either sensors/harvesters or actuators using the same active material. So far, Pb(Zr,Ti) O\_3 (PZT) has been the most studied piezoelectric material, particularly for actuators, due to its outstanding piezoelectric coefficients. These last years, CEA-Leti has been working on the development of sol-gel PZT thin films for MEMS devices. The integration of piezoelectric PZT thin films with silicon MEMS can fulfill many of the requirements of sensors and actuators functions in microsystems, as a result of the large displacements, high sensing functionality and high energy densities that can be obtained, compared to pure Si-MEMS.

In this paper, we report on the different ways of measuring piezoelectric coefficients. The most important piezoelectric coefficient for actuation is the indirect transverse coefficient d31. It is extracted from measuring the deflection, with a white light interferometer, of a processed membrane actuated by the PZT film. d31 is fitted by using a Finite Element Model (Comsol), knowing PZT film mechanical properties such as Young's modulus (E) and Poisson's ratio (v). However, these elastic constants are not well known, that makes difficult the accurate determination of d31 piezoelectric coefficient. We have recently shown that Young's modulus (E) and Poisson's ratio (v) can be accurately characterized by Picosecond Ultrasonics (PU). This technique consists in the use of femtosecond optical pulses generated by a laser. The so-called pump pulse generates the propagation of both out-of-plane and transversal acoustic waves (Fig.1).

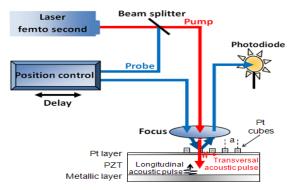


Figure 1: Picosecond Ultrasonics schematic set-up.

Knowing the PZT thickness allows us to calculate the longitudinal and transverse acoustic velocities in the PZT (cL and cT). Finally, we can extract E and  $\nu$  from the acoustic velocities using the theory of elasticity. We find E=82.1GPa and  $\nu$  =0.39 for the (100)-oriented 2µm-thick sol gel PZT film [1]. The extracted PZT d31 piezoelectric coefficient is 165±25 pm/V; which is among the highest values ever reported for PZT thin films.

The effective direct transverse coefficient e31,eff is also of interest for actuator applications. It can be extracted on cut pieces by using the 4-points bending system provided by Aixacct. In addition, double beam laser interferometry (DBLI) is a proven technique for the wafer level characterization of the effective longitudinal piezoelectric coefficient (d33,f) of thin films for industrial applications. The true d33,f is measured when the electrode pad size is equal to the substrate thickness for silicon substrate (Fig.2). For large pad sizes the measured d33,f reaches a saturated value which is significantly larger than the true d33,f. Our partners have found from a combined theoretical analysis and finite element model simulations that the difference between the saturation value of d33,f and the true d33,f is related to e31,f through the known elastic properties of the substrate [2]. A good agreement between e31,f derived from d33,f measurement and measurements of the same film using the 4-point bending method on cut pieces is obtained. A value of -19.1 C/m<sup>2</sup> is extracted from large signal measurements.

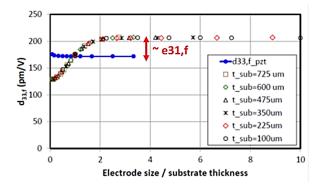


Figure 2: d33,f measurement by DBLI.

As a conclusion, both coefficients (d33,f and e31,f) can now be simultaneously determined from a single non-destructive measurement technique (DBLI) at the wafer level without the need of full MEMS processing.

<sup>[1]</sup> F. Casset *et al.*, " Caractérisation des propriétés élastiques du PZT déposé en couches minces par acoustique picoseconde ", *Congrès Français d'Acoustique*, 22-25 avril 2014, Poitiers, France.

<sup>[2]</sup> T. Schmitz-Kempen et al., "Concurrent measurement of longitudinal and transversal piezoelectric coefficients on wafer-level by double-beam laser interferometry", 4<sup>th</sup> International Workshop on Piezoelectric MEMS (PiezoMEMS 2014), Oct. 28-29, 2014, Kobe, Japan.



# **MEMS Actuators for Haptic Applications**

# Research topics: PZT, Actuators, Haptic

F. Casset, G. Le Rhun, C. Dieppedale, B. Desloges, P. Renaux, JS. Danel, C. Chappaz (STM), S. Basrour (TIMA), S. Fanget

# Partnership: STMicroelectronics, TIMA Sponsorship: FUI-TouchIt

The tremendous development of tactile interface in many customers' applications such as smartphone or tablet PC leads industrials to study "haptic interfaces" or "touch screen" solutions which allow the user to interact with its environment by the sense of touch. This technology is already used but with limitations such as high power consumption and limited feedback effect (simple vibration). Sol-gel  $Pb(Zr_{0.52},Ti_{0.48})O_3$  (PZT) thin-film is a good candidate for many actuator applications due to its high piezoelectric coefficient. In particular, it can be used for haptic interfaces to create squeeze-film effect. It consists in changing the friction between the finger and a plate resonator. It provides high granularity level of haptic sensation, using low power consumption compared to existing solutions [1].

We already proved that the maximum substrate displacement amplitude of our haptic plate can be obtain by taking the deformed shape of the selected mode into account, and matching the actuators position with the substrate maximum displacement amplitude (Fig.1). PZT actuators promote the desired mode by bimorph effect. In particular, we studied 3 actuator configurations: 1 actuator column, 2 in-phase actuator columns separated by a wavelength and 2 in-phase actuator columns located at the extremities of the plate. Using FEM approach, we proved that two actuator columns separated by a wavelength induce the highest substrate displacement amplitude for both  $60\times40$  and  $40\times30$  mm² plates.

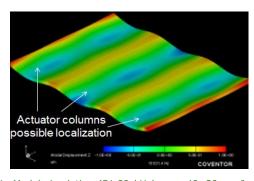


Figure 1: Modal simulation (51.89 kHz) on a  $40\times30$  mm² plate and PZT actuator column possible localization.

A generic technology, compatible with RF MEMS or loudspeakers, was used to build demonstrators. The piezoelectric stack consists of  $2\mu m$  thick sol-gel PZT in between 100nm thick Pt bottom electrode and 100nm thick Ru top electrode (Fig.2).

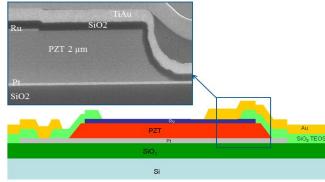


Figure 2: Schematic and SEM cross section of the technological stack.

Optical measurements were performed using a laser vibrometer (POLYTEC) by applying a dc-ac mixed voltage to the top electrode of plates ( $60\times40$  or  $40\times30$  mm²). Laser vibrometer measurements give the substrate displacement amplitude for a given actuation voltage. As shown in Fig.3, measurement results obtained using 12Vdc + 4Vac/peak-to-peak, in good agreement with simulation, indicates that 2 actuator columns separated from each other by a wavelength allow obtaining the highest substrate displacement amplitude [2].

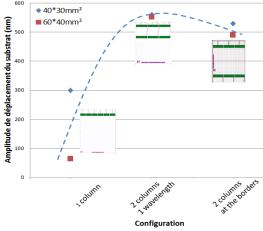


Figure 3: Laser vibrometer measurements -Substrate vertical displacement amplitudes on  $60\times40$  and  $40\times30$  mm<sup>2</sup> plate presenting various actuator configurations (12Vdc+4Vac/pp).

Finally, micrometric displacement amplitude, namely  $1.1\mu m$ , was obtained using only 8V ac. A haptic feedback effect was felt with the finger on this plate by using an actuation signal modulated at 10 Hz in amplitude.

#### Related Publications:

[1] F. Casset, JS. Danel, C. Chappaz, S. Basrour, P. Renaux, M. Gorisse, C. Dieppedale, F. Bernard, S. Fanget, E. Defay, "Thin film PZT actuators for haptic applications", *Piezoelectric Micro & Nano Structures and their Applications Workshop*, Sept. 25-26, 2014, Blois, France. [2] F. Casset, JS. Danel, P. Renaux, C. Chappaz, G. Le Rhun, C. Dieppedale, M. Gorisse, S. Basrour, S. Fanget, P. Ancey, A. Devos, E. Defay, "Characterization and post simulation of thin-film PZT actuated plates for haptic applications", 15<sup>th</sup> IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE 2014), April 7-9, 2014, Ghent, Belgium.



# Highly-Doped Suspended Silicon Nanowires for Gas Sensing by Thermal Conductivity Monitoring

## Research topics: Silicon Nanowires, Gas sensing

J. Ruellan, K. Benedetto, L. Duraffourg, T. Alava

#### Sponsorship: CARNOT Funding, DGA

In the aim of developing versatile and sensitive gas sensors, many efforts have been concentrated in sensing the targeted gas mass upon binding on Micro and Nano-mechanical resonators. The microgravimetric approach holds many advantages but still requires the use of an additional functionalization layer to favor adsorption of different gases. Moreover the need for energy for actuation and motion detection tend to increase the overall required power budget. The nanometric thermal conductivity detector (nano-TCD)

The nanometric thermal conductivity detector (nano-TCD) we are developing is based on the measure of thermal exchanges between a silicon self-heating nanowire and the surrounding gas. The suspended nanowire as shown in Fig.1 is self-heated by Joule heating and its temperature stabilizes itself through radiation interaction with the surrounding flowing carrier gas [1].

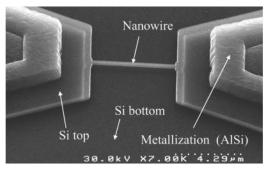


Figure 1: SEM micrograph of a single suspended silicon nanowire.

When an analyte gas to detect is mixed with the carrier gas. the thermal conductivity of the ensemble varies and induces a change of equilibrium for the self-heated nano-TCD. This equilibrium modification implies a change of temperature of the nanowire. Hence, we can measure change in thermal conductivity (i.e. therefore composition) of the surrounding gas by monitoring the nanowire temperature. Nano-TCDs have extremely low thermal time-constant, due to their very small sizes, which enables an AC-readout of temperature. Indeed, in this detection scheme, based on the commonly used 3-omega method, the nanowire is heated by an AC current leading to temperature variations at twice the frequency of the input signal (Fig.2). The mixing of the excitation current and the temperature-induced resistance variations leads to a signal at 3 times the frequency of the input signal [2].

The 3-omega output voltage is directly proportional to the temperature inside the nanowire. The temperature variations are given by the following equation:

$$\Delta T = \frac{1}{2} \frac{RI^2}{G_{th}}$$

Where R is the electrical resistance, I the excitation current and  $G_{th}$  the thermal conductance of the nanowire. Then, the amplitude of the third harmonic of the output voltage is given by the equation:

$$V_{3\omega} = \frac{1}{2} \Delta T \alpha R I$$

Where  $\alpha$  is the thermal coefficient of resistivity (TCR). This heterodyne transduction mode leads to a better signal-to-background ratio without requiring any differential setup. Moreover, operating with an AC detection reduces the flicker noise (which is the dominant noise in nanowires in DC mode) and leads to a better signal-to-noise ratio. Thanks to this method we aim at developing a low-cost, low-power high-resolution gas detector. Integrated along with a micro-preconcentrator and a micro-GC column the nano-TCD constitutes the core of a gas analyzer platform that is intended to detect ppm concentration of Hydrocarbon pollutant inside of surface water liquid samples with minimal integration space [2]. This is the goal of the GPS Carnot ALEC project executed in collaboration with the Division of technologies for biology and health within CEA-Leti.

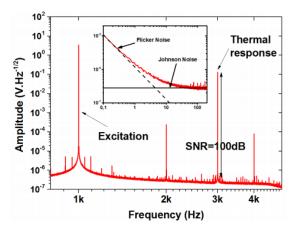


Figure 2 : Fast Fourier Transform of the voltage measured across the nanowire when heated by an AC current.

Related Publications:

[1] J. Ruellan, J. Arcamone, D. Mercier, C. Dupré, L. Duraffourg, "Pirani Gauge Based on Alternative Self-Heating of Silicon Nanowire", 17th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers & Eurosensors XXVII), June 16-20, 2013, Barcelona, Spain.

[2] J. Ruellan, J. Arcamone, M. Gely, T. Alava, L. Duraffourg, "Silicon Nanowire Based Thermal Conductivity Detector", *Eurosensors 2014*, Sept. 7-10 2014, Brescia, Italy.

[3] O. Martin, V. Gouttenoire, P. Villard, J. Arcamone, M. Petitjean, G. Billiot, J. Philippe, P. Puget, P. Andreucci, F. Ricoul, C. Dupré, L. Duraffourg, A. Bellemin-Comte, E. Ollier, E. Colinet, T. Ernst, "Modeling and design of a fully integrated gas analyzer using a µgC and NEMS sensors", Sensors and Actuators B: Chemical, Vol. 194, Pp. 220-228, 2014.

# Study on Linearity and Fatigue Resistance of Piezoresistive Nanogauges in M&NEMS Structures

#### Research topics: MEMS, NEMS, Nanogauge, Piezoresistivity, Fatigue, Linearity

P. Rey, G. Langfelder (POLIMI), A. Berthelot, G. Jourdan, P. Robert

# Partnership: POLIMI Sponsorship: FP7-NIRVANA

CEA-Leti has developed a new concept named M&NEMS. The basic idea is to combine in a same device, micrometric elements, sensitive to inertial force, with nanometric silicon nanowire strain gauges. The combination of nanometric elements within a surface micromachining MEMS process has proved to be a potential way to boost the performance of MEMS devices [1]. However, due to its dimensions (5µm long x 250nm in section), the nanogauge is often considered as the mechanical weak link of the structures. Experimental results on long-term reliability, fatigue and linearity of 250nm-thick crystalline silicon that can be used as piezoresistive sensing layer in inertial sensors are presented. Fatigue tests [2] were performed thanks to a specific bidirectional MEMS electrostatic actuator (Fig.1) able to apply high level stresses at different frequencies to a 250nm thick specimen with 700nm radius, such that the delivered force results in a stress concentration at its notch root. The electrostatic actuator is bidirectional: in this way the effects of different load ratios R defined as the ratio of the compressive to the tensile portion of the stress, compression taken as negative, can be observed. The structure displacement is monitored through a set of capacitive electrodes. In a first part of the experiment, 12 samples are led to single-cycle failure in order to evaluate the nominal tensile strength. The characteristic CV curve depends on the overall stiffness of the structure. A relatively large fraction of which ( $\sim$ 3%) being given by the nanometric specimen, the evidence of a failure is in the change of the characteristic curve.

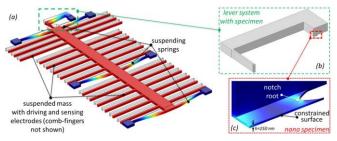


Figure 1: working principle of the test device: (a) the suspended mass (20 µm in thickness) applies – through a set of comb-finger actuators – a force to a lever system (b), which results in a stress concentrated at the notch root of a suitably designed specimen (c) with a thickness of 250nm.

The nanostructure shows a very high resistance. Yield tensile strength is found to be around 9GPa (i.e. 9 times higher than the value usually considered).

In a second part of the experiment, 13 samples are fatigued through sine waves well below the nominal tensile strength. The compressive and tensile displacements (in a ratio of about 80%) are continuously monitored. Fig.2 collects the

results, plotting the number of cycles to fatigue failure on the x-axis with respect to the maximum applied tensile stress on the y-axis (shown as a percentage of the found nominal tensile strength). Experimental points are fitted in terms of a Wöhler curve and compared to results on 15-µm and 22µm samples. It is demonstrated that the nanostructure can withstand 1 billion cycles at 4GPa. Lifetime at lower stress can be extrapolated: the nanostructure should be able to withstand 20 kHz cycles at a 1.1GPa stress level (i.e. 10 times the nominal stress used for the sensor full range) for 15 years.

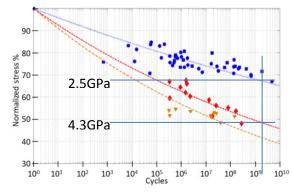


Figure 2: Wöhler curve showing the number of cycles before failure vs the stress expressed as a percentage of the yield strength. The blue points corresponds to a MEMS structure, red and orange points to a NEMS structure submitted respectively to tensile and compressive stress. Tensile strength for a MEMS structure (3.6GPa) being much lower than for a NEMS structure (9GPa), at a given number of cycles, the allowed stress level is much higher for the NEMS structure (or the number of cycles at a given stress that can withstand a nanostructure is higher).

The linearity study [3] is based on the same electrostatic actuator. The test specimen is now a nanogauge, 5µm long with a cross-section of (250 nm)². The results demonstrate a large linear range for tensile stresses (linearity errors below 5% up to 2.3GPa), and a lower linear range for compressive stresses (1.1GPa), this lower value being limited by buckling effect.

## Related Publications:

[1] P. Robert, V. Nguyen, S. Hentz, L. Duraffourg, G. Jourdan, J. Arcamone, S. Harrisson, "M&NEMS: A new approach for ultra-low cost 3D inertial sensor", 2009 IEEE Sensors, Oct. 25-28, 2009, Christchurch, USA.

[2] G. Langfelder, S. Dellea, P. Rey, A. Berthelot, A. Longoni, "Investigation of the fatigue origin and propagation in submicrometric silicon piezoresistive layers", 27<sup>th</sup> International Conference on Micro Electro Mechanical Systems (MEMS), Jan. 26-30, 2014, San Francisco, USA. [3] G. Langfelder, S. Dellea, N. Aresi, A. Longoni, "Linearity of Piezoresistive Nano-Gauges for MEMS sensors", Eurosensors 2014, Sept. 7-10 2014, Brescia, Italy.



# **Dual-Mode Probe for Ultrasonic Imaging and Therapy** based on cMUT Technology

#### Research topics: Microsystems, Electroacoustic Transducers, Ultrasound Imaging

C. Coutier, C. Dressler, B. Fain, M. Legros (VERMON), D. Gross (GREMAN), A. Bouakaz (INSERM), P. Vince (Althais), D. Certon (GREMAN)

## Partnership: VERMON, GREMAN, INSERM, Althaïs **Sponsorship: ANR-THERANOS**

The use of ultrasound techniques in the medical field has increased during the last decades, due to their non-invasive properties and ease of use at relatively low cost. For instance, novel modalities, such as focused ultrasound (FUS) for thermosensitive liposomal drug release or necrosis by hyperthermia, take benefit from the possibility to focus energy deep into the body. Among the research tracks to improve the quality of care is the adequate merging of different approaches within a unique system. The so-called theranostics combine the diagnostics and the therapy protocols to both image and treat the same region of interest. Ultrasound-based technologies also benefit from the progress in transducer design and fabrication. Capacitivemicromachined ultrasound transducer developed for more than twenty years offer promising features for medical systems, including a large bandwidth, a better impedance matching, a possible improvement of angular resolution and a simplified integration with the electronics. In particular, the reduced self-heating of cMUT is of great interest for FUS applications, since the required large and extended acoustic power impede the use of standard bulk piezoelectric transducer in this case.

In this context, the THERANOS project achieved a dual-mode probe for theranostics based on CMUT technologies. A whole system including PC controller, discrete electronics and CMUT transducers embedded within a pre-clinical probe was developed. Analytical analysis and specific numerical tools were used to define the probe specifications from the clinical need.

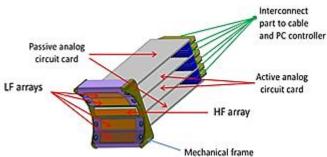


Figure 1: cMUT-based dual-mode probe.

A schematic view of the probe is presented in Fig.1. Four low frequency (LF - 1MHz) linear arrays were dedicated to the thermal activation of liposomes and a single high frequency array (HF - 16MHz) realizes simultaneous imaging of the insonified area. The LF arrays are positioned within a rigid frame in order to mechanically focus the acoustic power at a predefined distance from the transducer (20mm).

For this probe, CEA-Leti developed a patented "double gap" process flow to fabricate both LF and HF array on the same wafer, with the same process flow (Fig.2) [1]. Two etching steps allow to define two kinds of cavities with different gaps and sizes. The process is based on the direct wafer bonding of a SOI wafer, resulting in a high homogeneous membrane quality. The electric tests achieved at the element level reveal good inter-dies homogeneity, a low in-series resistance (R < 10  $\Omega$ ) and a coupling coefficient of 0.5 [2]. The collapse tensions, obtained by digital holographic microscopy, are typically 105V and 110V for LF and HF array respectively. Acoustic tests were also performed with a hydrophone, demonstrating that the output pressure can reach 200 kPa for a single LF array, which should result in a 4.5 MPa pressure at the focusing point. The cMUT bandwidth is measured at 136 %.

Finally, the imaging modality of the probe has been positively evaluated on a nylon-based phantom containing parallel polyethylene wire targets. The HF array is biased at 100V and excited by a bipolar pulse centered at 16 MHz (amplitude peak-to-peak: 80V). The position and size of the wire obtained after reconstruction match the corresponding simulations [3]. Additional developments are under progress to address in-vivo applications.

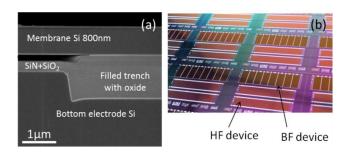


Figure 2: (a) cMUT cross-section obtained by scanning electron microscopy (b) Optical view of the devices before dicing.

#### Related Publications:

[1] D. Gross, C. Coutier, M. Legros, M. Perroteau, D. Certon, "Fabrication and characterization of wafer-bonded cMUT arrays dedicated to HF-ultrasound-image-guided FÜS", 13<sup>th</sup> Intern. Workshop on Micromachined Ultrasonic Transducers (MUT 2014), May 20-21, 2014, Copenhaghen, Denmark.

[2] D. Gross, M. Perroteau, D. Certon, C. Coutier, M. Legros, "Fabrication and characterization of wafer-bonded cMUT arrays dedicated to ultrasound-image-guided FUS", *IEEE International Ultrasonics Symposium (IUS 2014)*, Sept. 3-6, 2014, Chicago, USA.
[3] D. Certon, M. Legros, D. Gross, Ph. Vince, F. Gens, J.M. Grégoire, C. Coutier, A. Novell, A. Bouakaz, "Ultrasound pre-clinical Platform for

Diagnosis and Targeted Therapy", IEEE International Ultrasonics Symposium (IUS 2014), Sept. 3-6, 2014, Chicago, USA.







Thermal Management in 3D Stack

Recent Results on Stress Compensation for Thin Silicon Chips and Stress Sensors

Polymer Developments for 3D ICs

Interconnects by Cu-SiO2 Direct Hybrid Bonding: Low and High Temperature Behavior of Copper-Copper Structures

Electromigration in Hybrid Bonding (Cu/SiO2) Interconnects

High Vacuum Wafer Level Packaging for High-Value MEMS Applications

Biocompatible and Bio Stable Encapsulation for the Packaging of Medical Implantable Microsystem Devices



#### **Thermal Management in 3D Stack**

#### Research topics: 3D Integration, Thermal Management, Heat Spreader, Hot Spot

J.P. Colonna, P. Coudrain (STM), P. Vivet, F. de Crecy, P.M. Souare (STM), C. Santos, R. Prieto (STM), S. Cheramy

#### Partnership: STMicroelectronics

Thermal dissipation is a major concern in 3D circuits where the dense stacking of thin silicon layers leads to a significant increase of heat fluxes. Indeed, 3D integration offers a better space distribution management, improves signal speed and computing performances but it also increases heat fluxes in a reduced volume with new thermal resistances due to bonding between dies. Heterogeneous 3D integration must also take into account the different operating temperature of each individual die. A successful application of 3D integration in products will therefore require significant thermal analysis and establishment of thermal design guidelines.

For this purpose, a specific 3D thermal test chip has been developed at CEA-Leti in collaboration with STMicroelectronics [1]. It is composed of thinned top and bottom dies interconnected with Through Silicon Vias (TSVs) and  $\mu$ -bumps, stacked on a Ball Grid Array (BGA) substrate as shown in Fig.1.

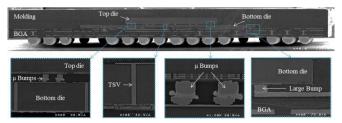


Figure 1: SEM cross section of the thermal chip.

Both dies have heating elements and numerous embedded temperature sensors. Thermal mapping has been performed with a large set of 3D interconnect configurations associated with various heating scenarios. A finite element modeling (FEM) strategy has been conducted in parallel to provide a calibrated and predictive tool able to simulate any scenario of 3D configurations with minimal error. Based on both experimental measurement and explorations with the FEM model, thermal recommendations have been presented in the scope of three important concerns for 3D circuit design and fabrication: design partitioning, inter-tier connections and package parameters. Design partitioning on the tiers controls the power pattern of the chip and may lead to generation of localized hotspots. Package parameters have a major influence like dies thicknesses. Silicon thickness is reduced to ensure acceptable TSV aspect ratio, but this thinning is detrimental to thermal dissipation. Finally, the thermal impact of 3D interconnects such as TSV and bumps has been investigated. The  $\mu$ -bumps can be used to create a thermal path between dies as shown in Fig.2. With µ-bumps the hot spot is no longer confined in the bottom die only and can spread in the top die.

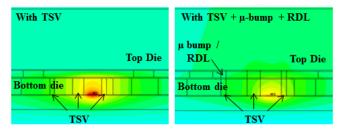


Figure 2: Temperature mapping with TSV only (left) vs TSV + RDL  $+\mu$ -bumps (right).

The thermal impact of TSVs has been analyzed in a dedicated study [2]. This study confirms the common thought that having TSVs in the silicon substrate increases the equivalent vertical thermal conductivity but it also shows that the insulation oxide around TSVs causes a lateral thermal blockage effect, especially for fine TSV pitches (Fig.3). It is demonstrated experimentally that the temperature of a localized hotspot is increased in the presence of TSVs due to the reduction of the lateral heat spreading capacity.

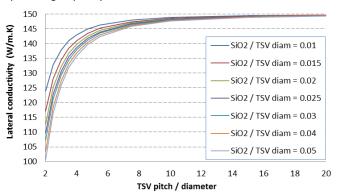


Figure 3: Reduced lateral thermal conductivity in silicon due to the presence of TSVs with different insulation oxide thicknesses.

In addition to thermal characterization, passive thermal dissipation has been investigated. The implementation of heat spreaders appears as one of the most suitable alternative for compact packages due to their ease of manufacturing and low cost. The performance of a high thermal conductivity layer integrated at die level has been demonstrated in the scope of short term industrial implementation [3]. Temperature reductions over 40°C have been measured for the best case scenario, with a thermal resistance enhancement of 61% at the die stack level. Finite volume simulations have also been performed in order to explain the thermal flux of the system.

#### Related Publications:

[1] P. M. Souare et al., "A Comprehensive Platform for Thermal Studies in TSV-based 3D Integrated Circuits", International Electron
Devices Meeting (IEDM 2014), Dec. 15-17, 2014, San Francisco, USA

Devices Meeting (IEDM 2014), Dec. 15-17, 2014, San Francisco, USA.
[2] C. Santos et al., "Using TSVs for Thermal Mitigation in 3D Circuits: Wish and Truth", IEEE International Conference on 3D System Integration (3DIC 2014), Dec. 1-3, 2014, Cork, Ireland.

[3] Ř. Prietò *et al.*, "Assessment of a Heat Spreading Solution for Hot Spots Cooling in Compact Packages", 20<sup>th</sup> International Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2014), Sept. 24-26, 2014, Greenwich, London, UK.



## Recent Results on Stress Compensation for Thin Silicon Chips and Stress sensors

#### Research topics: 3D Integration, Interposers, Stress, Characterization

G. Parès, P. Chausse, L. Vignoud

## Partnership: CERN, Glasgow University, STMicroelectronics Sponsorship: IRT Nanoelec.

3D integration is an enabling technology to realize high-performance and low-cost system on chip (SIP) by vertically stacking several functional dies. Such integration goes with a strong reduction of the chip silicon substrates which implies major warpage issues. At CEA-Leti we are currently developing a broad expertize on this topic based on experimental works coupled with simulation and theoretical approaches. Two recent achievements are illustrated in this report.

#### Stress compensation layer:

The pixel modules are the fundamental building blocks of the ATLAS pixel detector system used in CERN LHC facility. They consist in their basic form of a silicon sensor that is flipchipped bonded to a CMOS read-out integrated circuit (ROIC). One of the main objectives for ATLAS experiment is to develop an approach towards low mass modules and thus reducing radiation scattering. From the module perspective this can be achieved by using advanced 3D technology processes that includes the formation of Cu/SnAg microbumps on top of the ROIC front-side for the 3D connection, the thinning of both the sensor and the CMOS ROIC and finally the flip chip assembly of the 2 chips. The thinning of the silicon chips leads to low bump yield at the solder reflow stage due to bad co-planarity of the two chips creating dead zones within the pixel array. In the case of the ROIC, which is thinned to 100um, the chip bow varies from -100 µm at room temperature to +175 µm at reflow temperature resulting from CTE mismatch between materials in the CMOS stack and the silicon substrate. To compensate dynamically the stress of the front side stack a compensating layer is added onto the back-side of the wafer while it is still supported on its temporary carrier used for thinning. Utilizing our material thermo-mechanical database coupled with a proprietary analytical simulator "sigmapeps" and measuring the bow of the ROIC at die level we are able to determine an optimized layer stack. As shown in Fig.1 the bow magnitude can be reduced by approximately a factor of 4 by the introduction of the compensating layer consisting of the back side deposition of a SiN/Al:Si stack at low temperature. The amplitude of the correction can be managed by the deposition conditions and the thicknesses of the SiN/AI:Si stack.

Further development of the compensation layer stack using other couple of materials are on-going to reduce further the bow offset at room temperature as well as reducing the bow magnitude throughout the full solder reflow temperature range hence achieving high bump yield. In particular, this approach can also be combined with the introduction of a via-last technology in the pixel module architecture which will constitute a major achievement toward a more compact and more efficient detector.

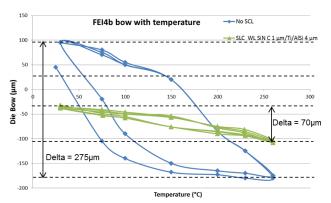


Figure 1: Effect of stress compensation layer on ROIC chip bow during temperature cycle.

#### Passive stress sensors:

Passive stress sensors have been integrated in a silicon interposer test vehicle to investigate thermo-mechanical stress in a typical 2.5D system. These sensors are integrated in a rosette-shape consisting of eight oriented copper serpentines acting like strain gauges (Fig.2). An innovative design theoretically allows the calculation of a partial stress tensor, including three planar and one out-of-plane components. Electrical measurements at wafer level, combined to FIB/SEM cross-sections revealed a strong impact of elaboration processes on the electrical response. Numerical simulations using finite element analysis were built to evaluate the theoretical sensitivity of copper serpentine to mechanical strains. Finally a dedicated fourpoint bending tool coupled with a four-terminal resistance measurement setup was fabricated to experimentally extract the values of sensors sensitivity factors (Fig.3). Results highlight a stress sensitivity of distinctly oriented resistors. Several identified sources of data dispersion are inherent to this measurement configuration and prevent a reliable calculation of strain gauges so-called "gauge factors".



Figure 2: Microscope view of the passive stress sensor.



Figure 3: Description of four-point bending set-up.

#### Related Publications:

[1] G. Pares, T. McMullen, S. Tomé, L. Vignoud, R. Bates, C. Buttar, " Development of a stress compensation layer for thin pixel modules 3D assembly", 47<sup>th</sup> International Symposium on Microelectronics (IMAPS 2014), Oct. 13-16, 2014, San Diego, USA.

[2] B. Vianne, P. Bar, V. Fiori, S. Gallois-Garreignot, K.A. Ewuame, P. Chausse, S. Escoubas, N. Hotellier, O. Thomas, "Thermo-mechanical Characterization of Passive Stress Sensors in Si interposer", 15<sup>th</sup> IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE 2014), April 7-9, 2014, Ghent, Belgium.



#### **Polymer Developments for 3D ICs**

#### Research topics: Underfill, Molding, Temporary Bonding, RF Characterization

A. Garnier, A. Jouve, Y. Sinquin, R. Franiatte, S. Cheramy, F. Fournel, Y. Lamy, O. El Bouayadi, Y. Lamy, T. Lacrevaz<sup>1</sup>, C. Bermond<sup>1</sup>, K. Vial<sup>2</sup>, R. Prieto<sup>3</sup>, S. Cheramy

#### Partnership: IMEP-LAHC<sup>1</sup>, EVG group<sup>2</sup>, STMicroelectronics<sup>3</sup> Sponsorship: IRT Nanoelec

3D integration relies on semiconductor chips assembly with vertical interconnections. To make it possible, polymer materials have to be implemented at different stages. For instance, the underfill (UF) is placed between the stacked chips to protect inter chips interconnections and enhance their reliability. On the other hand, Wafer Level Overmolding (WLOM) is used to encapsulate chips stacked on an interposer wafer which enables to decrease the packaging costs compared to a classical "molding last" approach. Additionally, WLOM is also a technological way to achieve a "chip stack first" approach: after stacking the chips on a thick wafer (the future interposer), it is used to fill the lateral gaps between de chips to make possible surface flattening in order to proceed with interposer backside processing. This latter step, a standard one in 3D integration is possible thanks to temporary bonding which involves polymers compatible with bonding and debonding.

Different kinds of UF were studied [1]: capillary UF (CUF), non-conductive paste (NCP, see Fig.1) and wafer level UF (WLUF). CUF has been the commonly used technique for years but is not suitable for high interconnect density and large chips. Compared to CUF, NCP and WLUF stand for good candidates in fine pitch needs ( $<50\mu m$ ). However, both are prone to UF entrapment and need to improve the process throughput. Although NCP is more mature than WLUF, the latter best fit thinner chips thanks to limited creeping. The choice between these techniques mainly depends on chip size, interconnection size and pitch, and process throughput requirements.

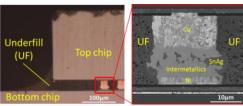


Figure 1: Cross-section views of 3D stack using NCP underfill with a close-up view of microbump solder joint (FIB image).

In wireless RF modules, 3D integration is a way to reduce the package size. In order to meet radiation specifications, one 3D approach is for instance to use reflective cavities (see Fig.2). In that case, a molding material (WLOM in the study) is required as a passivation layer. Its wideband frequency characterization relies on coplanar transmission lines directly integrated on the interposer [2]. The extracted WLOM properties (relative permittivity = 3.7, tangent loss = 0.07) have shown good correlation with supplier data and retro-simulation results and demonstrated the suitability of this material for our RF applications.

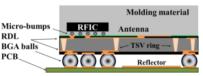


Figure 2: schematic view of RF module 3D stack with molding material on top of the interposer.

In [3], WLOM integration was assessed on a "chip stack first approach" (see Fig.3). A test vehicle simulating  ${\sim}100\mu m$  thick chips stacked on a 300mm wafer was laminated with two kinds of polymers, epoxy and silicone based. Best results were obtained with epoxy polymer but large wafer bow after lamination remains the main issue. Silicone polymer could reduce the stress but has to be tuned in order to completely fill the gap between the chips.

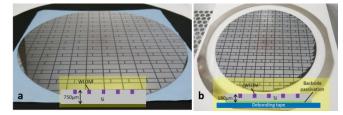


Figure 3: 300mm wafers with WLOM (a) after WLOM lamination and thinning, (b) after backside process and debonding on tape.

Finally, temporary bonding allows performing bonding with high topography strong enough for device thinning, backside processes and debonding from carrier to tape. In order to clearly understand the different bonding mechanisms, mechanical behavior of the two main polymer families (thermoplastic and cross linked) has been studied [4]. Fig.4 shows the possibility for the thermoplastic material to allow a mechanical decoupling between the carrier and the thin device during thermal treatment. This allows us to tune accurately the temporary bonding processes.

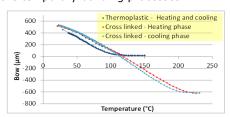


Figure 4: Bow measurement depending on the temperature of a bond pair processed with thermoplastic or cross-linked material.

Finally, polymer development is essential to overcome 3D integration challenges, from fine pitch interconnection chip stacking to WLOM integration for RF or "chip stack first approach", including temporary bonding process.

#### Related Publications:

[1] A. Garnier, A. Jouve, R. Franiatte, S. Cheramy, "Underfilling techniques comparison in 3D CtW stacking approach", *IEEE 64<sup>th</sup> Electronic Components and Technology Conference (ECTC)*, May 27-30, 2014, Orlando, USA.

[2] T. Lacrevaz et al., "Electrical Broadband Characterization Method of Dielectric Molding in 3-D IC and results", IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 9, Pp. 1515-1522, 2014.

[3] Y. Sinquin, A. Garnier, M. Argoud, A. Jouve, L. Baud, J. Dechamp, N. Allouti, S. Cheramy, "Molding materials performances experimental study for the 3D interposer scheme", *MiNaPAD Forum 2014*, May 20-22, 2014, Grenoble, France.

[4] K. Vial, F. Fournel, M. Wimplinger, J. Burggraf, M. Schachinger, J. Bravin, M. Pellat, "Mechanical coupling in temporary bonding", MiNaPAD Forum 2014, May 20-22, 2014, Grenoble, France.



#### Interconnects by Cu-SiO<sub>2</sub> Direct Hybrid Bonding: Low and High Temperature Behavior of Copper-Copper Structures

#### Research topics: 3D integration, Hybrid Bonding, Metallic Bonding

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## Partnership: STMicroelectronics, SOITEC, SIMaP Sponsorship: DGA, DGCIS, IRT Nanoelec.

Cu–SiO $_2$  direct hybrid bonding is considered as one of the most promising approaches for matching the needs of three dimensional integrated circuits (3D-IC). Results of a complete morphological, electrical and reliability study conducted on four-layer copper structures realized by Cu–SiO2 direct hybrid bonding has been shown (Fig.1). Ultrafine pitch 7 $\mu$ m, 3 $\mu$ m  $\times$  3 $\mu$ m pads daisy chains with up to 30 160 connections are bonded with submicron accuracy, matching the interconnection needs in upcoming 3D circuits.

A special attention was paid on the annealing temperature influence regarding to the bonding quality and electrical performances. The first key-parameter for adhesion at room temperature is linked to surface topology offers by advanced polishing process like CMP. In fact, the first challenge is lowering roughness to values compatible with hybrid direct bonding [1,2]. Moreover, bonding strengthening for copper surfaces exhibiting same surface topology properties was studied in the low temperature range [2]. Two process parameters were shown as predominant on post bonding annealing from 20°C to 100°C: bonding atmosphere and copper deposition technique. Indeed, bonding toughness increase in this temperature range seems to be linked to copper oxidation at bonding interface. On one hand, the water amount available when surfaces are brought into contact has a key role in this oxidation mechanism: bonding performed under a high relative humidity reveals higher strengthening kinetic. On the other hand, copper layers deposited by different technics shown different oxidation kinetics which lead to different mechanical strengthening behavior. Confirmed by phenomenon activation energy calculation, ECD deposition technique was designated as the best way to obtained high toughness assembly.

Beyond 300°C, bonded structures involving copper layers exhibit typical voids [1,3]. In order to have a better understanding of the voiding process, we designed specific structures (materials and surfaces) showing different properties [3]. These stacks underwent different bonding processes which mainly differ in the external applied load (Fig.2). For each experimental variation (material or bonding process) the total volume of voids was significantly different. Thus, we demonstrated that voiding phenomena in coppercopper direct bonding (Fig.2b) is related to a stress driven vacancy diffusion very comparable to standard metallurgical creep mechanisms. Regarding the origin of the vacancies, among all the possible options, two predominant sources have been identified: standard creep due to plastic deformation of copper layers due to external uniaxial pressure applied and tensile stress induced by silicon substrates on encapsulated copper layers. Oxide presence at bonding interface leads to a stress gradient creation which promotes vacancy accumulation at the edges of this phase.

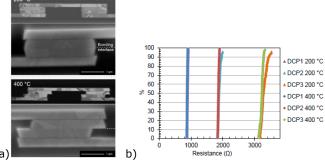


Figure 1: Daisy chain connection annealed at 200 and 400 °C for 2 h a) SEM cross sections. b) Cumulative percentage of the resistance of different daisy chains type. [1]

Along with these non-critical voids present at the bonding interface, electrical characterizations have proven that an annealing at 200 °C is sufficient to obtain outstanding electrical performance and functional yields. A thermal treatment at 400 °C offered the best results though, including a state-of-the-art contact resistivity of 120  $\rm m\Omega.\mu m^2.$  Additionally, most of the daisy chain structures successfully passed the environmental reliability tests, demonstrating the excellent resistance to corrosion and mechanical robustness of the four-layer high density daisy chains.

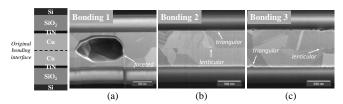


Figure 2: SEM cross section of copper bonded layers of structures dedicated to roughness effect. a- Bonding1 (high roughness + external pressure bonding). Faceted voids located at original bonding interface and at TiN-Cu interface. b- Bonding2 (low roughness + direct bonding). Lenticular voids located at the bonding interface. Triangular voids confined at the TiN-Cu interface. c- Bonding3 (low roughness + external pressure bonding). Higher density of lenticular and triangular voids than for Bonding2. [3]

Finally, electromigration studies [1] have shown that fully bonded copper lines with two layers behave like bulk interconnects with TiN and TaN/Ta barriers, as the Cu/Cu bonding interface does not introduce any new failure mechanism.

#### Related Publications:

[1] Y. Beilliard et al., "Advances Toward Reliable High Density Cu–Cu Interconnects by Cu–SiO<sub>2</sub> Direct Hybrid Bonding", *IEEE International Conference on 3D System Integration (3DIC 2014)*, Dec. 1-3, 2014, Cork, Ireland.

Conference on 3D System Integration (3DIC 2014), Dec. 1-3, 2014, Cork, Ireland.
[2] P. Gondcharton, B. Imbert, L. Benaissa, V. Carron, M. Verdier, "Kinetics of low temperature direct copper-copper bonding", Microsystem Technologies (2015), 21:995-1001.

[3] P. Gondcharton, B. Imbert, L. Benaissa, M. Verdier, "Voiding Phenomena in Copper-Copper Bonded Structures: Role of Creep", ECS Journal of Solid State Science and Technology, 2015 4(3):p77-p82.



#### Electromigration in Hybrid Bonding (Cu/SiO<sub>2</sub>) Interconnects

#### Research topics: Reliability, Electromigration, Copper, Hybrid Bonding, 3D

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Partnership: STMicroelectronics Sponsorship: IRT Nanoelec.

For high performance devices, interconnect pitch below 3  $\mu$ m is required and hybrid bonding integration scheme seems to be the solution. However, a lot of questions have to be answered regarding the compatibility of the direct bonding process and integration with a full industrial process flow, the electrical performances and the reliability [1].

In the present study [2], the reliability aspect is discussed from the electromigration point of view. Electromigration (EM) is always a major reliability concern of interconnects due to the aggressive scaling of their dimensions and the ever increasing current densities. The EM phenomenon is an atomic flow driven by the electrons and enhanced by temperature and thermo-mechanical stresses. Roughly speaking, at the anode side, voids nucleate and grow, and ultimately lead to an open interconnect. At the opposite, at the cathode side, extrusions can be observable leading to potential short circuit risk if conductive lines are close enough.

The hybrid bonding process flow consists in a 200 mm wafer-to-wafer (WtW) bonding including two copper lines (one per wafer). Each wafer is previously processed identically as described hereafter. After trench opening into a deposited  $SiO_2$  layer, barrier (TaN/Ta or TiN) and Cu seed layers are deposited. Copper (ECD) filling is carried out and annealed at 400 °C for microstructure stabilization purpose. After an optimized CMP, wafers are bonded at room temperature (alignment precision: < 1  $\mu$ m), atmospheric pressure and ambient air. A 400 °C post bonding anneal is then applied in order to strengthen the bonding. To allow a direct electrical probing, several steps are performed on the bonded wafers: top wafer thinning (< ~55  $\mu$ m), TSV etching, Cu redistribution layer (RDL)/organic passivation and underbump metallization (UBM) deposition.

For the present study, the barrier is a TaN/Ta one. NIST-like test structures are used for electromigration (EM) tests. Two configurations are designed in order to investigate the role of the bonding interface and more precisely its nature (Cu-Cu or Cu-oxide) on the EM resistance: a fully bonded one and a partially bonded one. EM tests are performed at package level. Electrical resistance is monitored through four-point sensing during EM test. Resistance measurements performed during EM tests show a first latency period during which the resistance remains constant, followed by first a progressive and then an abrupt increase.

Failure analyses were carried out on all samples and typical EM defects were detected: voids and extrusions (see figures 1-2). Extrusions consist in interfacial whiskers at the oxide/oxide interface as illustrated in Fig.1-b. The failure mechanism is mainly dominated by a void nucleation at the  $Cu/SiO_2$  interface and more rarely at Cu/barrier interface.

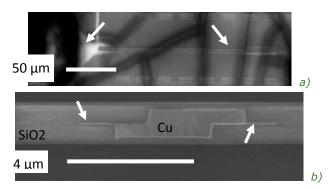


Figure 1: Extrusion after electromigration tests on hybrid bonding test structures, a) top (IR imaging) and b) cross-section (ionic imaging) views.



Figure 2: Voids after electromigration tests on hybrid bonding test structures, top view (IR imaging).

Regarding the statistical analysis, after the elimination of extrinsic and early failures, both test structures have unimodal distributions with similar standard deviations confirming that the failure, in all cases, is due to the same failure mechanism activated by current and temperature with common activation energy and current exponent. In this respect, the activation energy is estimated at 1±0.15 eV and  $0.7\pm0.14~\text{eV}$  for fully and partially bonded test structures respectively. The difference between both test structures from the activation energy point of view can be simply attributed to the surface of Cu-Cu or Cu-SiO<sub>2</sub> interface. Therefore, it appears that the larger the Cu-Cu bonding surface is, the larger is the activation energy. The current exponent has a value of 0.87±0.2 and 1±0.23 respectively for fully bonded and partially bonded configuration, values are in good agreement with the theoretical value of 1 for a growth time dominated failure.

To conclude, EM tests performed on a Cu direct bonding interconnects reveal excellent and comparable performances to BEoL ones. Additional EM studies are ongoing with different types of integration (different chemistries of copper and barrier), post-annealing conditions in order to find the best integration scheme. In situ EM characterizations are also in progress in order to have a clear overview of the failure mechanism and define a predictive numerical model.

Related Publications:

[1] Y. Beilliard et al., "Advances Toward Reliable High Density Cu–Cu Interconnects by Cu–SiO2 Direct Hybrid Bonding", IEEE International Conference on 3D System Integration (3DIC 2014), Dec. 1-3, 2014, Cork, Ireland.

[2] S. Moreau et al., "Mass transport-induced failure in direct copper (Cu) bonding interconnects for 3-D integration", 2014 IEEE International Reliability Physics Symposium (IRPS 2014), June 1-5, 2014, Waikoloa, HI, USA.



# High Vacuum Wafer Level Packaging for High-Value MEMS Applications

#### Research topics: MEMS Wafer Level Packaging, Vacuum, Hermeticity, Getter

S. Nicolas, F. Greco, S. Caplet, C. Coutier, C. Dressler, M. Audoin, X. Baillin, G.Dehag, F. Souchon, S. Fanget

#### Partnership: SERCEL

The packaging of MEMS at the wafer level has been a field of interest for many years now and large panel of solutions are available.

In this area, MEMS devices dedicated to consumer market generally required hermetic package with "medium" vacuum level (up to  $10^{\text{-}1}$  mbar). On the other hand, for high-value applications, with components such as high precision gyroscope or µbolometer, high vacuum level (below  $10^{\text{-}3}$  mbar) is mandatory. Such high vacuum level remains difficult to achieve and to control due to phenomenon like leak, outgassing, permeation and moreover, it generally requires a thin film getter.

In the past years, results with vacuum close to  $10^{-3}$  mbar have already been published with Chip Scale Packaging (CSP) technologies, for µbolometer application as an example. But, to the best of our knowledge, very little works have been published about such high vacuum level obtained with Wafer Level Packaging (WLP) technologies.

Our previous reported works on anodic bonding showed that a vacuum level of  $10^{-2}$  mbar could be obtained after TSV integration. At that time, our conclusion was that outgassing phenomenon has to be understood to explain the rise of the residual pressure during the TSV process.

This work addresses the development of a high vacuum wafer level packaging technology that targeted vacuum level below  $10^{-3}$  mbar. For this purpose, a silicon resonator has been used and combined with an optimized AuSi eutectic bonding solution. The final structure after packaging with eutectic bonding is reported on Fig.1.



Figure 1: MEMS structure after vacuum WLP with eutectic bonding.

To estimate the residual pressure inside the cavity the Q factor of the resonator is measured after packaging. The well-known theoretical model showed that the Q factor is inversely proportional to the residual pressure inside the cavity. But the model also exhibits a strong dependence of the Q factor with the resonator's design. Thus, the theoretical curve Q factor vs residual pressure could be obtained but some approximations have to be done.

In order to be as close as possible from our final MEMS structure, an experimental set-up has been carried out to measure the Q factor in function of the residual pressure. The pressure inside the chamber has been tuned from  $10^{\text{-1}}$  to  $10^{\text{-5}}$  mbar and Q factor has been measured (Fig.2).

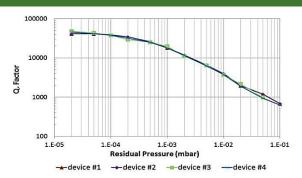


Figure 2: Q Factor vs Residual pressure – experimental results on 4 functional devices.

Considering that outgassing effects during bonding are mainly responsible for the residual pressure degradation and by making the assumption that the getter material is not fully saturated after bonding, a specific bonding recipe has been optimized.

Furthermore, different getter sizes have been implemented with covering surface representing 5 to 50 % of the original cavity surface.

Mean Q factor and mean residual pressure are reported on Fig.3 for four different getter sizes.

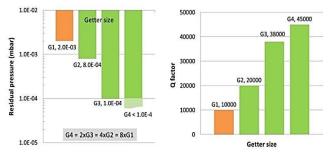


Figure 3: Residual pressure and Mean Q factor vs getter size – Optimized eutectic bonding & getter activation process.

As expected, mean Q factor increased with getter size and a mean residual pressure of  $10^{-4}$  mbar has been obtained with larger getter surfaces (G3 & G4). It has to be noticed that for G4, it is not possible to have an accurate estimation of the residual pressure since measured residual pressure are below the sensitivity range of our resonator ( $10^{-1}$  to  $10^{-4}$  mbar).

Finally, we have demonstrated that with an eutectic bonding solution, residual pressure below  $10^{-3}$  mbar could be obtained with a yield higher than 80%. It has even been demonstrated that residual pressure down to  $10^{-4}$  mbar could be obtained which is, to our best knowledge, a high-level achievement in the vacuum wafer level packaging area.

#### Related Publications:

[1] S. Nicolas, F. Greco, S. Caplet, C. Coutier, C. Dressler, M. Audoin, X. Baillin, G. Dehag, F. Souchon, S. Fanget, "High vacuum wafer level packaging for high-value MEMS applications", 2014 IEEE 64<sup>th</sup> Electronic Components and Technology Conference (ECTC), May 27-30, 2014, Orlando, USA.



### Biocompatible and Bio Stable Encapsulation for the Packaging of Medical Implantable Microsystem Devices

#### Research topics: Medical Devices, Bio-Packaging, Microsystem

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### Partnership: SORIN Group Sponsorship: OSEO Innovation

The miniaturization of microsystem offers new opportunities for medical applications. Gradually, the electronic devices that were previously external invade the human body in order to improve therapy or physiological parameter measurements. However, human body is a new environment for such devices and two main issues have to be considered. First of all the body has to be preserved from toxic elements of the device and secondly, electronics parts have to be preserved from corrosive substances which constitute the major part of the body.

The CEA-Leti, in partnership with SORIN Group, develops a cardiac implantable device which measures endocardial acceleration signal [1]. The electronic components are attached on a wafer silicon interposer and encapsulated in a wafer silicon lid which is bonded using eutectic AuSi. The process is performed at the wafer level (Fig.1).

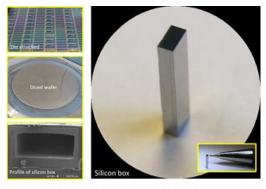


Figure 1: View of silicon cardiac implantable package.

The silicon box is finally connected to the electrical generator outside the heart thanks to two conducting wires. The gas content and hermeticity of the package were analyzed using different techniques such as Residual Gas Analysis with helium, argon or krypton 85 testing. RGA analysis allows the access to our cavity gas content and provides an estimation of water standard leak rate. The water standard leak rate was estimated to  $\sim$ 6  $10^{-13}$  atm.cc/s which guarantees a life time much more than 20 years [2].

Moreover, the Food and Drug Administration (FDA) requires as well that whenever novel Si devices are used inside a medical device, they must be coated with a biostable and biocompatible encapsulant which acts as bi-directional barrier to the diffusion of toxic or corrosive substances from or into the device [3]. In addition, it should be compatible with the manufacturing process flow of silicon devices in standard clean rooms in order for this technology to be economically interesting. Candidate materials such as  $Al_2O_3$ ,  $HfO_2$ ,  $TiO_2$ , ZnO, SiN,  $SiO_2$ , SiOC, SiC, a-CH, and BN were evaluated.

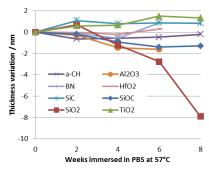


Figure 2: Thickness variation of different packaging layers immersed in  $57^{\circ}\text{C PBS}$ .

Our screening methodology consisted in evaluating selected packaging layers based on:

- Accelerated aging tests (Fig.2) in a saline solution that simulates the chemical environment present inside the human blood serum, such as Phosphate-Buffer Saline (PBS).
- Gas permeability tests to assess the hermetic seal of the packaging layers to external agents such as moisture or oxygen.
- Cytotoxicity and morphology tests to confirm the biocompatibility of the selected layer.

It was found that widely used packaging layers in microelectronics such as SiN and SiO $_2$  are corroded by PBS at 37°C. Corrosion rates in 37°C PBS of 20-100nm/yr and 0.5-1.2  $\mu m/yr$  are expected for SiO2 and SiN packaging layers deposited by PECVD at 400°C, respectively. SiO2 has good properties as gas barrier and it does not have a very high corrosion rate. Therefore, for some short-term applications that are not in direct contact with chemically aggressive biofluids, the use of PECVD-deposited SiO $_2$  might be a solution.

ZnO packaging layers have stability problems after a couple of days of PBS immersion. Adhesion problems between ALD-deposited ZnO layers and the native oxide surface of Si wafers are suspected.

Packaging layers of  $Al_2O_3$ , a-CH, BN, HfO<sub>2</sub>, SiC, SiOC, and TiO<sub>2</sub> present good stability as shown by a film thickness variation smaller than 2nm after 6-8 weeks of immersion in PBS at 57°C. Moreover, four of them were confirmed to be non-cytotoxic according to in-vitro tests outlined by the norm ISO10993-5. They are consequently good candidates for biocompatible packaging layers of medical electronic devices that are in contact with chemically aggressive environments.

#### Related Publications:

[1] J-C Souriau *et al.*, "Implantable Device Including a MEMS Accelerometer and an ASIC Chip Encapsulated in a Hermetic Silicon Box for Measurement of Cardiac Physiological Parameter ", 2014 IEEE 64<sup>th</sup> Electronic Components and Technology Conference (ECTC), May 27-30, 2014, Orlando, USA.

[2] J-C Souriau *et al.*, "Characterization of a hermetic silicon box fitted in a cardiac lead in order to measure the endocardial acceleration signal", 5<sup>th</sup> Electronics System-Integration Technology Conference (ESTC), Sept. 16-18, 2014, Helsinki, Finland.

[3] J. M. H. Morales *et al.*, "Biophysicochemical Evaluation of Passivation Layers for the Packaging of Silicon Microsystems in Medical Devices", 2014 IEEE 64<sup>th</sup> Electronic Components and Technology Conference (ECTC), May 27-30, 2014, Orlando, USA.





Non-Destructive Characterization of Deeply Buried Interfaces of Gate Stacks Studied in "Integration-like" Conditions

Ultra-Low Traces Analysis of Noble Metals Contamination on Si-Wafers by VPD-DC-ICPM

Synchrotron Radiation based Characterization for Micro and Nanotechnologies

XPEEM Surface Microscopy for Investigating Local Properties of Novel 2D-Semiconducting Materials

Progress in Atom Probe Tomography for Semiconductor Analysis

Ultimate Sensitivity and Spatial Resolution for Strain Imaging using Precession Diffraction in a Transmission Electron Microscope

Nanometrology for Surface Functionalization Processes for the Production of Bio-Tech & Health Sensors

X-Ray Techniques for Non-Destructive Chemical Depth Profiling of Nanolayered Systems

Speeding up X-Ray Nanotomography for 3D Integration



## Non-Destructive Characterization of Deeply Buried Interfaces of Gate Stacks Studied in "Integration-Like" Conditions

#### Research topics: Gate Last, XPS, Nano-Characterization

P. Risterucci, O. Renault, E. Martinez, B. Detlefs, V. Delaye

## Partnership: ESRF, INL, U. of Southern Denmark Sponsorship: RTB Program

The International Technology Roadmap for Semiconductors (ITRS) specifies in its 2013 issue the need for developing non-destructive characterization techniques suitable for a better account of the material properties changes (for instance, the elemental depth distribution) in real device structures as a function of processing conditions. For example, in advanced CMOS nodes, it would be desirable to study the in-depth distribution of the active layers of the gate stack, such as the high-k and the control La layer, without deprocessing the top poly-Si gate.

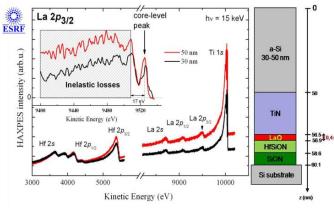


Figure 1: HAXPES survey spectra of gate stacks analyzed in integration-like conditions, showing the spectral fingerprint of the deeply buried La layer and its corresponding energy-loss structures [2] (ESRF, ID32, no longer in operation).

X-ray photoelectron spectroscopy (XPS) has proven over the last decades to be suitable for characterizing ultra-thin materials and elemental depth distribution within at the nm scale. However, the surface sensitivity of XPS (originating from the limited mean-free path of the characteristic photoelectrons travelling within the material) does not enable to probe deeper below the surface. Therefore, the material of interest is often studied in non-integration like conditions after deprocessing of the thick overlayer. The mean-path can be increased by using hard x-rays provided by synchrotron radiation sources and so-called Hard X-ray Photoelectron Spectroscopy (HAXPES), but the characteristic probing depth of the element-specific, core-level electrons is still limited to about 25nm. This does not enable to probe deeply buried interfaces as often encountered technological device structures.

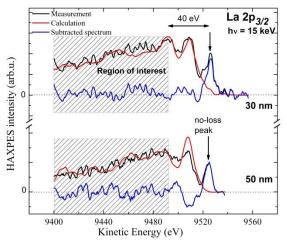


Figure 2: Inelastic background modelling of the La2p3/2 core-level in full gate stacks with 30 and 50 nm poly-Si top gate. The top La/TiN interface is found at 41 nm (resp. 57 nm) with a 30 nm-thick Si cap (resp. 50 nm-thick) [1].

We got around this limitation by considering the energy-loss structures of HAXPES spectra which appear to lower kinetic energy than the core-level peak (Fig.1). In XPS the shape of the energy-loss signal, or inelastic background, can be analyzed in a quantitative way to retrieve accurately relative changes in the depth distribution of a particular element, using the so-called Tougaard algorithm. To assess the sensitivity of the Tougaard method in HAXPES, we have studied typical gate stack structures without deprocessing the top poly-Si gate (either 30 or 50nm-thick) prepared in a gate-first integration approach on 300 mm Si wafers at ST-Microelectronics. Transmission Electron Microscopy (TEM) confirmed the thickness of the poly-Si gate, whereas EELS profiles measured the La thickness to be about 1nm. We have successfully implemented the Tougaard's method on the La inelastic background (Fig.2) [1]. We therefore reproduce the position of the top La interface by our modelling. The depth over which La is found to extend depends on the poly-Si overlayer thickness: it is 4nm in the case of a 50nm-thick gate, and decreases steadily to the expected value of 1nm as the overlayer thickness gets smaller (30nm and 20nm) [2]. In conclusion, we have implemented a novel, generic method enabling the nondestructive quantitative analysis of deeply buried interfaces, and applied this to high-k/metal gate stacks studied in integration-like conditions.

#### Related Publications:

[1] P. Risterucci, O. Renault, E. Martinez, B. Detlefs, V. Delaye, J. Zegenhagen, C. Gaumer, G. Grenet, S. Tougaard, "Probing deeper by hard x-ray photoelectron spectroscopy", *Applied Physics Letters*, Vol.104, Issue 5, n° 051608, 2014.
[2] P. Risterucci, O. Renault, E. Martinez, B. Detlefs, J. Zegenhagen, G. Grenet, S. Tougaard, "Inelastic background analysis of HAXPES

[2] P. Risterucci, O. Renault, E. Martinez, B. Detiefs, J. Zegenhagen, G. Grenet, S. Tougaard, "Inelastic background analysis of HAXPE spectra: towards enhanced bulk sensitivity in photoemission", *Surface and Interface Analysis*, Vol. 46, Issue 10-11, Pp. 906-910, 2014.



## Ultra-Low Traces Analysis of Noble Metals Contamination on Si-Wafers by VPD-DC-ICPMS

#### Research topics: Metallic Contamination, Noble Metals, Chemical Collection-Model

H. Fontaine, M. Devita (STM), N. Drogue (STM), D. Mathiot (Icube Lab), V. Enyedi, T. Lardin, S. Cetre

Partnership: STMicroelectronics, ICube Laboratory Sponsorship: Nano2017

Nowadays, noble metals are largely introduced in advanced nanoelectronic devices (as Pt silicide), in N&MEMS or in heterogeneous integration (Au, Ag, Ru, Ir...). dissemination along the manufacturing line represents a critical contamination issue for Si-wafers in reason of their high potential of detrimental impacts. Hence, their control is required at very stringent contamination levels, lower than  $1.10^{+10}$  at/cm<sup>2</sup> and even  $1.10^{+8}$  at/cm<sup>2</sup> depending on the technology, representing then a big metrology challenge. The Total reflection X-ray Fluorescence (TXRF) technique does not allow the measurement of noble elements at lower levels than 1.10<sup>+11</sup> at/cm<sup>2</sup> whereas the very sensitive (up to  $10^{+7} - 10^{+8}$ at/cm<sup>2</sup>) and accurate HF Vapor Decomposition-Droplet Collection (VPD-DC) of metallic contaminants followed by the droplet solution analysis with Inductively Coupled Plasma Mass spectrometer (ICPMS) is not applicable. Indeed, the usual acidic solutions used for the collection droplet (based on HF, HNO<sub>3</sub>, H<sub>2</sub>O<sub>2</sub> mixtures) are inefficient for the noble metals due to their high oxidoreduction potentials.

In this context, the implementation of a VPD-DC-ICPMS analysis for Au, Pt, Ag, Pd, Ru and Ir was addressed using a specific droplet solution based on a diluted HF/ Aqua Regia (AR= mixture of HNO $_3$  and HCl) chemistry selected for its high oxidant and complexing power. The development was investigated from an automatic VPD-DC tool (Rigaku VSEE300) using intentional contaminated wafers at controlled doses from few  $10^{+9}$  to  $10^{+13}$  at/cm $^2$ . Both ionic-form and metal-form contaminations were considered in order to cover different chemical states.

Main operational factors governing the collection efficiency (CE) of noble metals such as HF/AR chemistry composition, droplet scan speed, VPD step duration... were optimized from intentional contaminated wafers [1,2] both for a bevel and full surface analysis. Then, comprehensive data of collection rates depending on the contaminant dose (from few 10<sup>+9</sup> to  $10^{+13}\ \text{at/cm}^2)$  and the area scanned by the droplet were established. Results show that Pt, Pd, and Au in ionic-form and Ru in metal-form present a collection decrease with the contaminant dose and the scanned wafer area. This dose and scan area dependency on the VPD-DC seems to mean that the chemical activity (i.e. the collection power) of the droplet falls along the process due to droplet interactions both with Si-wafer and/or contaminants. For other elements, CE is higher than 75% and not dependent on these factors. Anyway, these results highlight that for levels lower than  $1.10^{+11}$  at/cm<sup>2</sup> collection efficiencies are higher than 60% allowing a relevant analysis in this low concentrations range. Then, Low Limits of Detection were determined confirming the very high expected sensitivity of this technique (see Table 1).

element	Ag	Au	Ir	Pd	Pt	Ru
full surface	1	0,9	0,6	1	6	2
bevel	45	51	17	38	180	58

Table 1: Low Limits of Detection (LLDs) of noble metals on 200mm Si wafers by VPD-DC-ICPMS (x 10+8 at/cm²).

CE results were completed by a surface characterization along the VPD-DC steps performed on ionic-form contaminated wafers. Then, the evolution along the DC process of the oxide thickness, AFM roughness and SEM observation correlated to the CE dependency on the dose and scanned area allow us to propose a droplet collection model based on simultaneous processes of oxidation-desoxidation of the Si surface and reduction-oxidation of the noble contaminants (see Fig.1) [1].

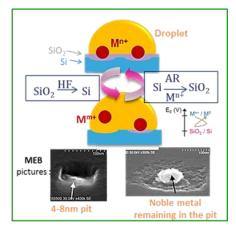


Figure 1: Scheme of the proposed collection model based on simultaneous processes of oxidation-desoxidation of Si and reduction-oxidation of noble metals.

In conclusion, the very high sensitive analysis of noble metals ( $\sim 1.10^{+8}$  at/cm²) by VPD-DC-ICPMS was successfully developed using a diluted HF/Aqua Regia chemistry allowing a satisfactory collection efficiency of the contaminants at lower levels ( $< 1.10^{+11}$  at/cm²). Moreover, the knowledge of the chemical collection mechanisms implied as the key operational parameters allow us to consider improvement perspectives of the technique and its application for in-line metrology.

#### Related Publications:

[1] M. Devita, H. Fontaine, N. Drogue, D. Mathiot, V. Enyedi, T. Lardin, "Improvements in VPD-DC for characterization of the noble metallic contamination on Si wafers", 2014 SEMATECH Surface Preparation and Cleaning Conference (SPCC), 22-24 April 2014, Austin, USA.
[2] M. Devita, H. Fontaine, N. Drogue, D. Mathiot, V. Enyedi, T. Lardin, "Collection efficiency of noble metallic contaminants on Si wafers with HF-Aqua Regia mixtures for VPD-DC ICPMS analysis", Solid State Phenomena, Vol. 219, pp 268-271, 2014.



# Synchrotron Radiation Based Characterization for Micro and Nanotechnologies

#### Research topics: X-Ray Analysis

#### P. Gergaud, P. Bleuet, N. Vaxelaire, G. Freychet, D. Ferreira Sanchez

#### Partnership: ESRF Sponsorship: ANR-AMOS, ANR-RTB

The brilliance of the x-ray beams produced on a synchrotron provides the micro-nano-technologies with a powerful probe of the structure, morphology and behavior of a wide range of materials. A large range of techniques is available: diffraction, diffusion, imaging, with spatial resolution at the nanoscale, time resolution during annealing, and energy tunability for enhancing anomalous effects. This is illustrated by the four examples below.

Nano-pencil beam x-ray diffraction (Fig.1a) [1]: A singlescan approach allowing evaluation of chemical and structural gradients in polycrystalline thin films with a resolution of tens of nanometers has been developed. Thinned samples are measured in cross section in a transmission geometry with a high-energy X-ray nano-pencil beam (100nm×50um). Powder diffraction methods can be used because of the strongly asymmetric beam shape (i.e. the large number of diffracting grains), allowing the solution of structural phases within the film thickness. For each phase, microstructural gradients such as strain, stress, texture and grain size are deduced from two-dimensional diffraction patterns. The efficiency of this approach is demonstrated on ferritic thin films, where the phase ratio and stress gradient (in each phase) have been successfully quantified with a 150nm depth resolution.

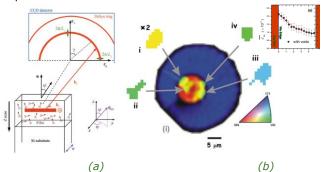


Figure 1: (a) Nano-pencil beam configuration for phase gradient analysis into a film; (b) Grains orientation into a Cu TSV deduced from micro-LT and radial strain gradient into the Si substrate.

Micro-beam Laue tomography (LT) (Fig.1b) [2]: Here, white X-ray micro-beam Laue diffraction is developed and applied to investigate elastic strain distributions in three-dimensional (3D) materials, more specifically, for the study of strain in Cu 10 um diameter–80 um deep through-silicon vias (TSVs). Two different approaches have been applied: (i) two-dimensional micro-Laue scanning and (ii) micro-beam Laue tomography. 2D micro-Laue scans provided the maps of the deviatoric strain tensor integrated along the via length over an array of TSVs in a 100 um thick sample prepared by Focused Ion Beam. The micro-beam Laue tomography analysis enabled to obtain the 3D grain and elemental

distribution of both Cu and Si. The position, size (about 3 um), shape, and orientation of Cu grains were obtained. Radial profiles of the equivalent deviatoric strain around the TSVs have been derived through both approaches. The results from both methods are compared and discussed.

GISAXS study of copolymer (BCP) films (Fig.2) [3]: The selfassembly (SA) of PS-b-PMMA copolymer (BCP) films, leading to hexagonal arrays of perpendicular PMMA cylinders in a PS matrix, and its ordering kinetics were investigated using ex situ and in situ grazing incidence small-angle X-ray scattering (GISAXS). The ex situ measurements have provided accurate information about the structural changes in SA BCP films with multiple processing parameters. The temperature-dependent GISAXS measurements indicate that phase-separation starts around 140 °C and annealing up to 240 °C is required to form homogeneous SA films within the short baking times required by industry. Furthermore, the so-called graphoepitaxy approach was also studied. The GISAXS pattern of the graphoepitaxial film reveals the formation of a single domain extended over large areas, in contrast with the pattern of the BCP film on unpatterned area showing randomly oriented domains.

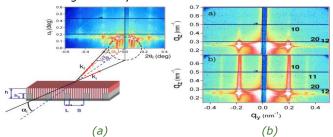


Figure 2: (a) GISAXS configuration (b) GISAXS patterns for Self Assembly of PS-b-PMMA films.

#### Anomalous SAXS on core-shell NPs [4]:

Suspensions of bimetallic nanoparticles (NPs) of Ru and Cu have been synthesized by simultaneous decomposition of two organometallic compounds in an ionic liquid. These suspensions characterized by Anomalous Small-Angle X-ray Scattering (ASAXS) at energies slightly below the Ru K-edge showed that the NPs adopt a Ru-core, a Cu-shell structure, with a constant Ru core diameter of 1.9nm for all Ru: Cu compositions, while the Cu shell thickness increases with Cu content up to 0.9nm. The formation of RuCuNPs thus proceeds through rapid decomposition of the Ru precursor into RuNPs of constant size followed by the reaction of the Cu precursor and agglomeration as a Cu shell. Thus, the different decomposition kinetics of precursors make possible the elaboration of core–shell NPs composed of two metals without chemical affinity.

#### Related Publications:

[1] N. Vaxelaire, P. Gergaud, G.B.M. Vaughan, "Sub-micrometer depth-gradient measurements of phase, strain and texture in polycrystalline thin films: a nano-pencil beam diffraction approach", *Journal of Applied Crystallography*, Vol. 47, pp. 495-504, 2014.
[2] D.F. Sanchez *et al.*, "X-ray  $\mu$ -Laue diffraction analysis of Cu through-silicon vias: A two-dimensional and three-dimensional study",

Journal of Applied Physics, Vol.116, Nb 16, ref. 163509, 2014.
[3] M. Maret et al., "Probing Self-Assembly of Cylindrical Morphology Block Copolymer Using in Situ and ex Situ Grazing Incidence Small-

Angle X-ray Scattering: The Attractive Case of Graphoepitaxy", *Macromolecules*, 47(20), pp. 7221–7229, 2014.
[4] I. Helgadottir, G. Freychet, P. Arquillière, M. Maret, P. Gergaud, P. H. Haumesser and C. C. Santini, "Ru-core/Cu-shell bimetallic nanoparticles with controlled size formed in one-pot synthesis", *Nanoscale*, 6(24), 14856-62, 2014.

#### XPEEM Surface Microscopy for Investigating Local Properties of **Novel 2D-Semiconducting Materials**

#### Research topics: 2D-Materials, Surface Characterization

O. Renault, H. Kim, D. Rouchon, D. Mariolle, J. Dijon, A. Tyurnina, J.-P. Simonato

#### **Partnership: CEA-Liten** Sponsorship: RTB Program, Flagship-GraFEn

The specific low-dimensionality of atomically-thin twodimensional (2D) semiconducting materials such as graphene gives to surface effects a dominant role in their properties in general. It also introduces new challenges in physical characterization. Due to the 2D-character of these materials, surface-sensitive techniques are particularly well suited, however the complexity of the phenomena involving 2D systems, such as doping, requires that these techniques are used in combination with many other ones able to provide complementary information (roughness, atomic structure) or to probe different lateral scales (AFM, TEM).

available surface-sensitive photoemission microscopy with XPEEM (X-ray Photoelectron Emission Microscopy) is particularly adapted. The first reason is because the study of 2D systems often implies to characterize single domains at the micron scale. The second reason comes from the complementary set of relevant information that XPEEM can provide: local work function, surface concentration and chemical state of the elements, electronic band structure.

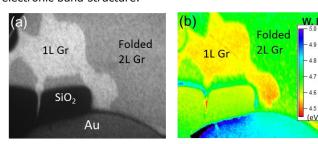


Figure 1: Threshold photoemission XPEEM image corresponding work function image (b) of CVD graphene (Gr) after iodine doping transferred onto patterned SiO2/Si.

Here, we illustrate the potentials of XPEEM combined with Raman spectroscopy in the particular case of lowtemperature, doped CVD graphene. Doping graphene through physisorption is a promising route as it can increase the charge carrier concentration without degradation of the carrier mobility, as in the case of chemisorbed dopants through covalent functionalization. We performed spectroscopic XPEEM with various excitation sources to assess the efficiency of p-doping by iodine physisorption on single- (1L) and randomly stacked (2L), strongly decoupled bilayer polycrystalline graphene domains (Fig.1a) [1].

The doping results in a work function increase of  $\sim 0.4-0.5$ eV (Fig.1b), with a higher degree of iodine uptake by the bilayer (2%) as compared to the single layer (1%), as shown by the XPEEM image of the surface iodine concentration in Fig.2a; this suggests iodine intercalation between two

graphene planes with a larger interlayer spacing (~ 5nm) as it is the case here on the folded 2L domain. The chemistry of iodine is identified consistently as I(3-) and I(5-) poly-iodide anionic complexes (Fig.2b) with slightly higher concentration of I(5-) in bilayer than monolayer graphene, likely attributed to differences in doping mechanisms. This is in agreement with an independent analysis using Raman spectroscopy (Fig.2c), which also confirms the absence of molecular iodine at the surface.

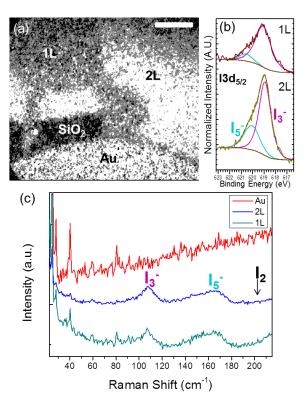


Figure 2: XPEEM image (scale bar: 15 μm) of the iodine surface concentration (a), at the same location as in Fig.1; corresponding I 3d core-level (b) and Raman spectra (c) on each domain, evidencing the chemistry of iodine adsorption/intercalation in the form of reduced complexes I(3-) and I(5-).

XPEEM is performed with a NanoESCA instrument (Omicron-Oxford Nanoscience) fitted with a laboratory x-Ray source (AlK alpha1).

#### Related Publications:

[1] H. Kim, O. Renault, A. Tyurnina, J.-P. Simonato, D. Rouchon, N. Chevalier, J. Dijon, "Doping efficiency of single and randomly stacked

bilayer graphene by iodine adsorption", *Applied Physics Letters*, Vol. 105, 011605, 2014.
[2] O. Renault, H. Kim, A. Tyurnina, D. Rouchon, N. Chevalier, J. Dijon, "Doping efficiency of single and randomly stacked bilayer graphene by iodine adsorption", 9<sup>th</sup> *International Workshop on LEEM-PEEM*, Sept. 14-18, 2014, Berlin, Germany.



#### **Progress in Atom Probe Tomography for Semiconductor Analysis**

#### Research topics: Electron Tomography, Atom Probe Tomography, GAA Transistor

A. Grenier, R. Serra, G. Audoit, D. Cooper, J.P. Barnes, S. Duguay (GPM), D. Blavette (GPM), F. Vurpillot (GPM)

### Partnership: UMR 6634 CNRS (GPM), STMicroelectronics Sponsorship: ANR-APTITUDE, RTB Program

The next CMOS generations for the 20nm and 14nm nodes will introduce new device architectures, FINFET or FDSOI transistors being the two main contenders. The development of these technologies will require characterization techniques capable of performing 3D imaging and chemical composition measurements at the atomic scale. Atom probe tomography (APT) is expected to be one of the tools of choice for 3D chemical analysis of current and future devices. APT gives the chemical mapping of atoms in three dimensions with a spatial resolution below 0.5nm.

In the present study, we have investigated the structural and chemical properties of advanced gate-all-around transistor to evaluate the 3D characterization capabilities of APT. These devices are based on square cross section Si nanowires obtained from a (100) SOI substrate after anisotropic etchings of the top Si layer on a 145nm buried oxide. The Si nanowire is surrounded by a high-k metal gate stack. The nominal gate stack for the GAA device consists of 1nm of SiO<sub>2</sub> (interlayer: IL), 3nm of HfO<sub>2</sub> (high-k), 10nm of TiN and 60nm of poly-silicon.

APT result of a single GAA is shown in Fig.1a, each dot represents one atom. The HKMG stack is identifiable, with discrimination between high-k and IL thanks to the spatial resolution of APT. However, the reconstructed volume shows strong deviations from the morphology observed by electron tomography. It should be noted that the chemical identification is not affected by these artefacts. The S-like shape is due to the deviation of the object from the tip axis.

Simulations of the evaporation of surface atoms have been performed to understand the origin of the distortions observed in the GAA reconstructed volume. They are based on a 3D numerical code and take into account the different evaporation fields of materials. The results of simulations demonstrate the direct impact of a higher evaporation field around lower evaporation field (Si channel) environment, leading to higher density on the detector of the Si channel. Local magnification effects due to the trajectory aberrations of the ions near the sample surface are the cause of these distortions and are responsible for image deformations.

Correlative microscopy combining both atom probe tomography and electron tomography (ET) can be used to minimize these issues for nm-scale transistors. The square cross-section of the Si nanowire is confirmed as it is shown by the 3D isosurface representation (Fig.1b) deduced from electron tomography analysis of the GAA structure. The threshold for the isosurface rendering has been set at the intensity level of the TiN encapsulating layer. In this case, the Si nanowire channel is not directly represented, but the location of its boundary is inferred from the shape of the

surrounding high-k layer. APT reconstructions have been improved using a density correction method. The average dimension of the nanowire determined by electron tomography experiments has been used to find the best fitting parameters for the APT reconstructions after the first order density corrections. These corrections only affect the local atomic density, whilst preserving the local composition in the image. The resulting reconstruction is presented in Fig.1c. Even if some important distortions remain, the shape and dimensions of the GAA transistor are now in good correlation with the dimensions measured by electron tomography. The quantification of each layer within the gate stack of GAA becomes possible [1].

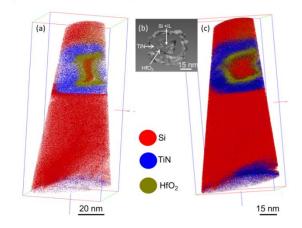


Figure 1: 3D APT volume based on standard reconstruction algorithm for GAA (a), isosurface rendering of GAA Si nanowire transistor deduced from electron tomography analysis (b), improved 3D APT reconstructed volumes based on atomic density correction (c).

In this case electron and atom probe tomography have been performed on different (but equivalent) samples made from the 3D transistor array. However performing electron tomography and APT on the same tip will be primordial to understand field evaporation and improve the reconstructions in order to obtain a full 3D characterization such as doping spatial distribution [2].

#### Related Publications:

[1] A. Grenier, S. Duguay J.P. Barnes, R. Serra, G. Haberfehlner, D. Cooper, F. Bertin, S. Barraud, G. Audoit, L. Arnoldi, E. Cadel, A. Chabli, F. Vurpillot, "3D analysis of advanced nano-devices using electron and atom probe tomography", *Ultramicroscopy*, Vol. 136, 2014.
[2] A. Grenier, S. Duguay, R. Serra, N. Rolland, G.Audoit, J.P. Barnes, J.P. Barnes, D. Cooper, F. Vurpillot, "Correlative atom probe and STEM-HAADF tomography of nanodevices", *Atom Probe Tomography&Microscopy* (APT&M2014), Aug.31–Sept.5, 2014, Stuttgart, Germany.



### **Ultimate Sensitivity and Spatial Resolution for Strain Imaging** using Precession Diffraction in a Transmission Electron Microscope

#### Research topics: Strain Engineering, Semiconductor Devices

N. Bernier, D. Cooper, M.P. Vigouroux, V. Delaye, G. Audoit, F. Bertin, J.L. Rouvière

#### Partnership: INAC, CNRS LTM, LMGP Sponsorship: LabEx-MINOS, ANR-AMOS

The advances in strain engineering must be supported by improvements in local strain characterization techniques to address the simulation, design and fabrication challenges faced by the semiconductor industry. Transmission electron microscopy (TEM) is the method of choice for nanoscale measurement of strain, however the existing techniques have serious limitations such as the poor strain sensitivity of 0.25% for high-resolution imaging. Despite significant development work [1], the difficulty of using dark field electron holography to analyze silicon-on-insulator (SOI) devices is due to the need to tilt the specimen which limits the spatial resolution in projection. Recently, J.L. Rouvière et al. [2] introduced the use of precession electron diffraction (PED) for strain measurement with 1nm spatial resolution and 0.02% sensitivity. PED is now intensively applied to ultra-scaled devices at the Nanocharacterization Platform (PFNC) on a double aberration corrected FEI Titan Ultimate microscope. This technique provides considerable insight into nanoscale strain engineering for a wide range of semiconductor technologies studied at CEA-Leti.

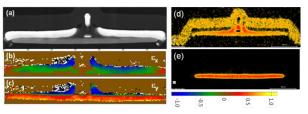


Figure 1 : (a) STEM image of the  $\Omega$ -Gate NW along the source/drain direction, (b-c) deformation mapping along the in-plane and growth directions, respectively, (d-e) Si and Ge concentration mappings (Ge content of the SiGe channel estimated to be ~30%).

A recent example regards the hybrid channel CMOS nanowires with SiGe p-FET and Si n-FET that have been successfully fabricated with diameter down to 7nm and 11nm gate length. In-depth electrical characterization evidenced higher p-FET performance (+90%) due to a compressive state in the SiGe channel as revealed by the PED analysis shown in Fig.1. Indeed, the strain distribution with high spatial resolution clearly evidences compressive strain along the in-plane direction in ultra-scaled nanowire (NW) width (here down to 12nm). This corroborates the p-FET performance increase evidenced in hybrid channel CMOS. For the first time, CEA-Leti together with SOITEC and STMicroelectronics showed that hybrid channel CMOS integration can be easily used with high efficiency for NWbased technology [3].

From combining experimental deformation maps measured by PED and finite element mechanical simulations, we have been able to quantify the stresses developed in a stressor Si<sub>3</sub>N<sub>4</sub> film. A specimen containing SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> dummy gates

with a gate length of 35nm and recessed SiGe sources and drains was examined by PED (Fig.2). Deformation maps for the x, xz, z directions, as well as the rotation have been acquired experimentally and these have been compared to simulations of the deformation which account for the relaxation of the specimen thin foil. The excellent signal to noise in the strain maps allows fine tuning of the parameters that are used in the simulations in order to provide a better fit, as proved in Fig.2. From the simulations it has been possible to derive a ~1.9 GPa stress developed in the nitride film which is an important property for semiconductor device design.

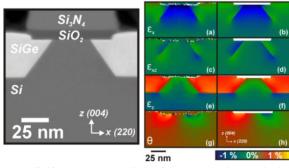


Figure 2: (left) STEM image of the dummy-gate device. (right) (a)-(d) Deformation maps of the device specimen acquired by precession diffraction for the x, xz, z directions and  $\theta$  respectively. (e)-(h) Comparison showing the best fitting simulated deformation maps.

To make the most of PED, this technique is implemented to non-corrected TEM's fitted with commercially available offaxis camera (such as the JEOL 2010FEF at the PFNC). M.P. Vigouroux et al. [4] showed that using an advanced diffraction pattern treatment a precision of ~0.03% with a probe size as small as 4.2nm is obtained on a conventional TEM. This method was applied to the study of the strain state in InGaAs quantum-well (QW) devices elaborated on Si substrate. As seen from Fig.3, results showed that the GaAs/Si mismatch does not induce in-plane strain fluctuations in the InGaAs QW region.

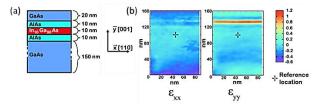


Figure 3: (a) GaAs/AlAs/InGaAs/AlAs/GaAs multi-layers grown on 300 mm Si (100) substrates; (b) exx, eyy strain mappings obtained by precession diffraction on a non-corrected TEM.

#### Related Publications:

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- [4] M.P. Vigouroux et al., "Strain mapping at the nanoscale using precession electron diffraction in transmission electron microscope with off axis camera", Applied Physics Letters, 105 (2014) 191906.



#### Nanometrology for Surface Functionalization Processes for the **Production of Bio-Tech & Health Sensors**

#### Research topics: Nanometrology, Surface Functionalization, AFM-CNT

C. Beitia, L. Robin, S. Marsaudon (CBMN), N. Chevalier, D. Mariolle, G. Nonglaton

#### Partnership: U. of Bordeaux, CBMN

In the nanotechnology bio-medical and health sector one of processes technological kev is the surface functionalization of materials that will serve to interact with molecules, proteins, bacteria and/or virus [1]. represents a global view of main steps in surface functionalization process flow. It clearly indicates the need for this process control: surface roughness; surface topography and chemical-biological functionalization. In this context AFM for roughness and topography will be a must. However concerning the chemical and the biological functionalization AFM alone is not enough. Indeed, a functionalization measurement requires not only nanometer resolution but as well chemical and biological specificity. Super-resolution fluorescence optical microscopy might be an alternative but it has two majors inconvenient: instrument is expensive and the measurement will require an additional process step to graft the luminophore molecule to the surface, which for production in-line control is not the best option. In this context, surface functionalization process metrology remains a challenge.

Over the last years, studies have been carried out in the feasibility of Frequency modulated AFM (FM-AFM) using carbon nanotube AFM probes (CNTP) to measure surface functionalization [2]. Indeed, AFM is available on most of Fabs and a CNTP has become more easily available [3]. From data analysis point of view, FM AFM has two major advantage, first it allows not only image topography measurement but at the same time it collects two additional channel the frequency shift by conservative forces and the damping due to dissipative forces. In addition the coupling with CNTP will take advantage of the amazing mechanical properties of CNT's and also has the possibility to be specific through chemical and biological grafting of the CNTP itself. In collaboration with CBMN measurements has been implemented at CEA-Leti and evaluated from metrology perspective. Fig.2 shows the first results. It illustrates for Silicon, Graphite and Silicon + Silane, the response of the CNTP in an approach-retreat curve.

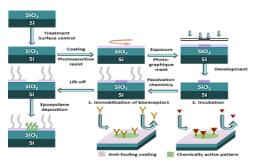


Figure 1: Functionalization process flow.

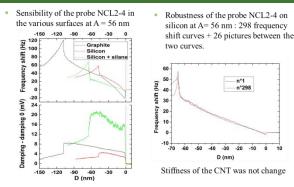
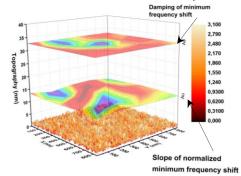


Figure 2: a) Surface sensitivity and b) robustness for FM-AFM CNTP measurements.

The mechanical properties of the CNTP, shows very different frequency shift response indicating a different interaction with the surface but also different damping process taken place since the damping response is not the same. It was confirmed after the measurement that the CNTP itself has not changed. Complementary to this, Fig.2b shows that spite of the fact of intensive use of the CNTP to do images and approach retreat curves the response does not change I a significant way.

Finally the multiple information's (topography, conservative and dissipative interactions) obtained might be used to study, the functionalization. Fig.3 displays map information linking topography (height); energy interaction (frequency shift) and energy dissipation (damping@ minima of frequency shift) over the surface [4]. Work is forecasted on getting more resolved maps to better match with the topography maps and analyzing the correlations between the channels over the surface. Reference measurements with metrology institutes in order to insure the trueness of measurements results as well as traceability will be done.



3: Channel information FM-AFM combination functionalization measurements.

Related Publications:
[1] Hoang A. et al, "Surface Functionalization for Micro- and Nanosystems: Application to Biosensors", in Chemistry in microelectronics,

editors Y. Le Tiec and R. Baptist, John Wiley & Sons, Inc., Hoboken, NJ USA, 2013.
[2] L.Robin *et al.*, "Pointe AFM à nanotube de carbone pour la métrologie in-line de procédés de fonctionnalisation de surface", *Forum des* 

Microscopie à sonde locale, March 17-21, 2014, Montauban, France.
[3] A.-S. Rollier et al., "High yield grafting of carbon nanotube on ultra-sharp silicon nanotips: Mechanical characterization and AFM imaging", IEEE International Conference on Micro Electro Mechanical Systems (MEMS), Jan. 21-25, 2007, Hyogo, Japan.

[4] L. Robin et al., "AFM Probe with Carbon Nanotube for the Metrology of Surface Functionalization", International Conference on Scanning Microscopy on Soft and Polymeric Materials (SPM-on-SPM), Sept. 2-6-2014, Toronto, Canada.



# X-ray Techniques for Non-Destructive Chemical Depth Profiling of Nanolayered Systems

#### Research topics: Metrology, X-ray Fluorescence, Chemical Depth Profiling

B. Detlefs, P. Hönicke (PTB), M. Müller (PTB), E. Nolot, H. Grampeix, B. Beckhoff (PTB)

### Partnership: Physikalisch-Technische Bundesanstalt, Berlin (PTB) Sponsorship: EMRP-TReND

Accurate physical-chemical characterization of composition and structure of thin layers and their interfaces is crucial to correlate functionality and process conditions in the development of new nanoelectronic devices. At the same time, the characterization presents a metrology challenge: analysis of very small amounts of material, often buried within the device stack; with material properties differing from the bulk ones which makes quantification based on reference materials impossible. X-ray-based elemental depth profiling methods combine elemental selectivity spectroscopic techniques with the structural sensitivity contained in the angular variation of the spectroscopic signal. Depending on the thickness of probed samples, X-ray fluorescence signal (XRF) or photoelectron spectroscopy (XPS) can be used as elemental probes.

Within the metrology EMRP-TReND project (Traceable characterization of nanoelectronic devices) we characterized elemental depth profiles of Al2O3/HfO2 nanolaminates by grazing incidence X-ray fluorescence spectroscopy (GIXRF) and parallel angle-resolved X-ray photoemission spectroscopy (PARXPS) in order to assess the accuracy and uncertainties of both methods.

Nanolaminate composite materials consisting of alternating layers of different materials with nanometer scale thickness may have physical properties very different from those of their constituents. Al $_2$ O $_3$ /HfO $_2$  nanolaminates with layer thickness in the nm range were shown to possess increased dielectric constant, high insulation characteristics and efficient charge trapping, properties with potential use in memory applications.

The samples were grown by atomic layer deposition (ALD) technique which provides uniform thin layers with low roughness and low intermixing at interfaces. Several bi-, triand multilayers were analyzed by GIXRF combined with Xreflectivity measurements (XRR). The fluorescence signal varies with the angle of incidence of the impinging X-rays not only because of changing attenuation within the stack but more importantly because of an amplification term that arises from interference between the incident and reflected X-ray beams. This factor improves significantly the sensitivity of the technique to variations in the depth profile. Elemental depth profiles are then reconstructed by optimization of both optical and structural parameters of the modelled stack. Use of XRR data in the combined analysis provides an independent assessment of these parameters translated into electron density profile [1].

Two X-ray excitation energies were used in the GIXRF experiment: 10 keV for accurate quantification of Hf signal (from Hf La emission) and 1622 eV for Al Ka fluorescence. These energies were chosen in order to reduce substrate signal and to reduce secondary and higher order excitation.

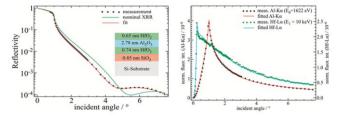


Figure 1: Comparison of a calculated XRR curve using tabulated optical constants for the sample shown in the inset and a fit to the measured XRR, optimizing only the optical constants (left panel). Comparison of the measured GIXRF angular fluorescence profiles for Al and Hf for the  $HfO_2/Al_2O_3/HfO_2$  trilayer and their best fits (right panel).

Experimental results and their best fits are shown in Fig.1. They illustrate the need for the combined analysis: not only the structural parameters but also densities and optical constants have to be fitted. We have shown that omission of this effect may lead to differences exceeding 5% in the evaluation of the amplification term resulting in errors of up to 20% in the GIXRF fit parameters, i.e. thickness and position of individual layers in the stack [2].

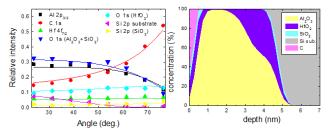


Figure 2: Angular dependence of XPS and its best fit (left panel) resulting in a concentration depth profile indicated in the right panel.

For comparison, the same samples were characterized by PARXPS, taking advantage of the chemical species sensitivity of XPS which allows us to separate oxide components. Despite different optimization approach, very good agreement between the in-depth profiles from several non-destructive depth-profiling techniques was found [3].

The experimental protocols and data analysis codes were developed primarily for the synchrotron applications. Work is in progress to adapt them for the characterization of more complex nanolayered structures, and for use with in-line metrology systems available at CEA-Leti.

#### Related Publications :

<sup>[1]</sup> M. Müller, P. Hönicke, B. Detlefs, C. Fleischmann, "Characterization of High-k Nanolayers by Grazing Incidence X-ray Spectrometry", *Materials*, Vol. 7, Issue 4, pp. 3147-3159, 2014.

<sup>[2]</sup> B. Detlefs, P. Hönicke, M. Müller, E. Nolot, H. Grampeix, B. Beckhoff, *European Conference on X-Ray Spectrometry (EXRS-2014)*, June 15-20, 2014, Bologna, Italy.

<sup>[3]</sup> P. Brüner, T. Grehl, H. Brongersma, B. Detlefs, E. Nolot, H. Grampeix, E. Steinbauer, P. Bauer, "Thin film analysis by low-energy ion scattering by use of TRBS simulations", J. Vac. Sci. Technol. 33 (2015) 01A122.



#### Speeding Up X-Ray Nanotomography for 3D Integration

#### Research topics: Through Silicon Vias, Copper Pillar, 3D Characterization

P. Bleuet, D. Laloum, T. Printemps

Partnership: STMicroelectronics, FEI
Sponsorship: STMicroelectronics, FEI, Catrene-Master3D

X-ray tomography is a well-established 3D characterization technique used to retrieve the 3D morphology of a sample from its 2D projections. This method is used in many fields, like medicine, non-destructive testing, pharmaceutical applications, material science or even security. Tomography is non-destructive and gives the 3D distribution of features like voids, porosities or heterogeneities in a sample. Despite its high-potential, this characterization method can be time-consuming: to fulfil the sampling criteria, it is necessary to record several hundreds of projections of the sample. Here we implemented and optimized a recent reconstruction algorithm based on the minimization of the total variation (so-called 'TVM') that makes it possible to record much less projections preserving a good, if not better, image quality.

The application is 3D integration in microelectronics, for which it is necessary to perform characterization of individual interconnects to better understand the metallurgy of copper pillars or image voids in TSVs. Since interconnects are 'big', e.g. 10-80 micrometers in diameter, electron imaging is not appropriate because it is too local and has a limited penetration depth.

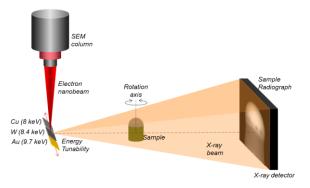


Figure 1: Experimental setup. The electron beam of an SEM illuminates a target which in turns produces x-rays.

For this purpose, we developed x-ray nanotomography hosted in a scanning electron microscope (Fig.1), thereby combining the high penetration depth of x-rays to a high spatial resolution, as already reported previously [1].

The interaction volume between the electron beam and the target is small enough to ensure a 100nm spatial resolution, though at the expense of the photon flux. For that reason, the initial scanning time was pretty long - typically a 24 h for a single silicon chunk containing 4 middle TSVs. To get rid of this, a basic strategy is to record less projections and to counterbalance by using advanced reconstruction algorithm

that are able to process few 2D radiographs to produce a 3D volume.

Reconstruction of a 3D volume from few 2D projections may lead to an infinite number of solutions. By assuming that the object to be reconstructed is sparse (in our case Si, Cu and air), an optimal solution can be found among the infinite number of solution by minimizing its L1-norm or the object gradients. This prior knowledge is sufficient to use 3 times less projections than usually, thereby reducing the scanning time by a factor 3, as shown on Fig.2 on TSVs [2]. We used and existed open-source package [3] to perform this work, that has been integrated in the data processing workflow.

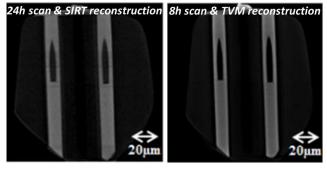


Figure 2: Frontal reconstruction through 2 voided TSVs. Left reconstruction is performed with the standard 'SIRT' algorithm and 190 projections while the right image shows a reconstruction with only 60 projections.

The 2 papers referenced hereafter [1,2] show some results on TSVs and copper pillars. On middle-TSVs, the total scanning time can now be reduced down to 8 hours. By increasing the last aperture of the SEM, we could also gain a factor of 2 in the x-ray intensity without resolution loss. In the case of copper pillars, it is still trickier to reduce the scanning time because the intermetallics contrast is poor.

With the current trend to lower the size of the microelectronics structures, new challenges come that motivate to reach higher spatial resolutions, i.e. to put more photons in smaller pixels. For that reason, hardware solutions have to be found. The next step, already under commissioning, is to increase the electron and x-ray brilliance and overall to improve the x-ray detection which is rather poor today. Last but not least, the energy is limited to 8-10keV so far and next plans include to move to hard x-ray nanotomography with energies of about 17-20keV. All this requires severe hardware modifications some of them being already executed.

#### Related Publications:

[1] D. Laloum, F. Lorut, J. Bertheau, G. Audoit, P. Bleuet, "Deep sub micrometer imaging of defects in copper pillars by X-ray tomography in a SEM", Micron 58, pp. 1–8, 2014.

[2] D. Laloum, T. Printemps, D. F. Sanchez, F. Lorut, G. Audoit, P. Bleuet, "Reduction of the scanning time by total variation minimization reconstruction for X-ray tomography in a SEM" , *Journal of Microscopy*, Vol. 256, Issue 2 2014, pp. 90–99.

[3] Palenstijn, W.J., Batenburg, K.J., Sijbers, J., "Performance improvements for iterative electron tomography reconstruction using graphics processing units (GPUs)", *Journal of Structural Biology*, Vol. 176, Issue 2, pp. 250-253, 2011.





MOCVD TiN Barrier to Copper Diffusion: a Solution for Very High Aspect Ratio TSV Metallization

Plasma Parameters Influence in PE(CVD/ALD) of Metal Nitrides on Insulators

Porous silicon based Maldi Platform for Medical Diagnosis
Ionic Liquids (ILs): an Innovative Medium for Nanofabrication

**Direct Bonding Mechanism** 



# MOCVD TiN Barrier to Copper Diffusion: a Solution for Very High Aspect Ratio TSV Metallization

#### Research topics: 3D, TSV, Deposition, MOCVD

T. Mourier, S. Minoret, L. Djomeni, S. Fadloun (SPTS)

Partnership: SPTS
Sponsorship: IRT Nanoelec.

In order to answer to integration specifications for 3D, requiring the metallization Through Silicon Vias (TSV) of aspect ratios higher than 10:1, replacement solution of widely used PVD TaN barriers have to be evaluated. Among potential MOCVD the candidates, Tetrakis(Diethylamino)Titanium (TDEAT) precursor appears to be the most attractive. The MOCVD barrier has been extensively studied at CEA-Leti for damascene integration but the deposition was usually performed at a temperature of 400°C which is not compatible with 3D TSV last integration requirements for which the maximum process temperature is limited to 200°C. For this reason, a new precursor was evaluated through a common laboratory with SPTS Diethylamino)Titanium Company and a CEA thesis [1]. It was installed on a new reactor designed for this precursor and a 200°C deposition capability delivered by SPTS. The process was developed on the Sigma FxP platform installed in the 300 mm 3D pilot line and integrated in the most advanced TSVs.

The primary work was done to fully characterize this material as a comparison with the existing 400°C TDMAT (Tetrakis(Dimethylamino)Titanium)based process developed for damascene but also as a specific material for a use in high aspect ratio structures. The physical properties of the deposited layer as shown on Fig.1 showed a low resistivity (350µohm.cm) comparable to TDMAT, a low compressive stress in the range of 500 MPa (compared to the 5GPa stress of PVD deposits) and a reasonable deposition rate of 20nm/mn. These values are compatible with a further transfer to mass volume production.

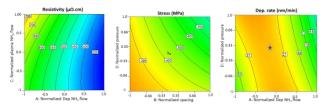


Figure 1: Resistivity, stress and dep rate of 200°C TDEAT TIN process.

Optimal process point was extensively characterized. Integrated diffusion properties were evaluated in  $10x80~\mu m$  TSVs using a newly developed characterization protocol allowing the copper profile measurement on the structure sidewalls [2]. The SIMS profiles showed no copper diffusion in the structure (Fig.2).

Step coverage is the key limitation for actual iPVD generation of barriers that appears to be limited to 10:1. The MOCVD coverage was analyzed for up to 20:1 A:R and showed a result of almost 30% for  $10x200\mu m$  TSVs to be compared to the nominal 3% coverage in  $10x100\mu m$  TSV obtained with PVD.

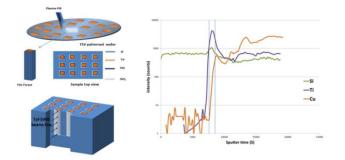


Figure 2: Integrated SIMS barrier efficiency measurement protocol.

Fig.3 shows the coverage MOCVD barrier in  $10x200\mu m$  deep features.

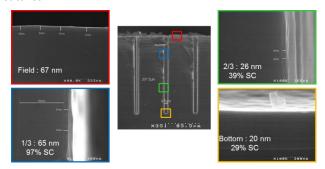


Figure 3: Step coverage of 60nm MOCVD TiN in 10x200µm TSV.

The layer was then integrated in a mid-process TSV structure with  $10x80~\mu m$  TSV and electrically measured. The Fig.4 shows the integration scheme and the electrical results for daisy chains up to 754 TSV. The TSV resistance is slightly lower than the one obtained for iPVD barrier and an excellent yield (>80%) is obtained [3].

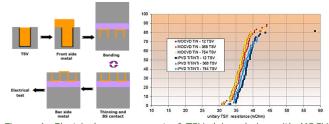


Figure 4: Electrical measurement of TSV daisy chains with MOCVD TIN.

The MOCVD TiN barrier was successfully developed in the frame of the common lab with SPTS and integrated in TSV structures and is now considered as the reference material for next generation 3D integrations.

#### Related Publications:

[1] L. Djomeni, "Etude de l'intégration des vias traversants réalisés par MOCVD en vue de l'empilement en 3D des composants microélectroniques", *PhD thesis*, Université de Strasbourg, 2014

[2]L. Djomeni et al., "Analysis of high aspect ratio Through Silicon Via (TSV) diffusion and stress impact profile during 3D advanced integration ",  $225^{th}$  ECS Meeting, May 11-15, 2014, Orlando, USA.

[3] L. Djomeni, T. Mourier, S. Minoret, S. Fadloun, F. Piallat, S. Burgess, A. Price, Y. Zhou, C. Jones, D. Mathiot, S. Maitrejean, "Study of low temperature MOCVD deposition of TiN barrier layer for copper diffusion in high aspect ratio through silicon vias", *Microelectronic Engineering*, Vol. 120, 25 May 2014, pp. 127–132.



#### Plasma Parameters Influence in PE(CVD/ALD) of Metal Nitrides on Insulators

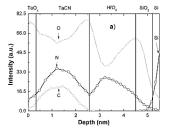
#### **Research topics: Advanced Materials**

R. Gassilloud, F. Piallat(STM), V. Beugin, P. Caubet (STM), C. Leroux, B. Pelissier (CNRS-LTM), C. Vallée (CNRS-LTM)

#### Partnership: STMicroelectronics, CNRS-LTM

Thorough understanding of metal electrodes composition and their interactions with insulators becomes more critical on advanced gate stack and emerging memories. Due to the relative chemical inertness of metal nitrides when deposited on  $HfO_2/SiO_2$ -InterLayer (IL), plasma enhanced (PE) chemical deposition of Titanium nitride (TiN) and Tantalum nitride (TaN) [1] are considered as very promising. Plasma dissociation and fragmentation of the precursor molecule affects the chemical, physical and electrical properties of the deposited film as well as the growth rate and conformity of the process. CEA-Leti has evaluated the impact of the plasma power during PEALD-TaN deposition on HfO2 sublayer and investigated the plasma induced precursor molecule fragmentation through frequency tuning during TiN deposition in PECVD mode. This work involves skills from the collaboration with CNRS-LTM through in-situ plasma diagnostic or in-line XPS characterization (IMPACT platform).

Complex species exchanges at nanometer scale are involved at metal/insulator interface. Fig.1 shows the depth composition profiles extracted by angle resolve X-Ray photoelectron spectroscopy (pAR-XPS) of PEALD-TaN deposited under low and high plasma radio frequency (RF) power conditions.



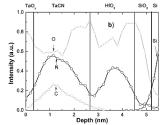


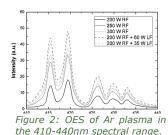
Figure 1: Depth profile reconstruction from AR-XPS of left: Low RF power TaN/HfO<sub>2</sub>/SiO<sub>2</sub> and right: high RF power PEALD-TaN/HfO<sub>2</sub>/SiO<sub>2</sub>.

The strong oxidation localized at TaN/HfO2 interface highlights the chemical interactions between the metal and the dielectric. N is not only limited to TaN layer; N is also localized in HfO2 layer. Nitrogen content in HfO2 layer presents a Gaussian shape, which can be explained by N migration into HfO2 activated by H2 plasma used during TaN deposition. High plasma power presents an accentuated distance between extrema compared to low power plasma. This difference implies that plasma power promotes N exchange from TaN to HfO<sub>2</sub> [2].

Another parameter, often not taken into account, is the plasma frequency. The plasma low frequency (LF at 350 kHz) addition to RF (13.56 MHz) can enhance the precursor

decomposition thanks to the modification of the plasma density. Fig.2 illustrates the effect of addition of LF to standard RF frequency on pure Argon plasma. In this figure, we compare the evolution of the intensity of the optical emission spectroscopy (OES, i.e. the plasma color) bands when going from low RF (200 W) to high RF (300 W) and from low RF to mix RF + 35 or 60 W LF. In both cases, an increase in the intensity was observed when increasing the power injected into the plasma. But it appears that higher intensities were obtained with LF addition while keeping a low 200 W RF power.

Consequently, in Fig.3 left, LF/RF mixed frequency strongly affects PECVD-TiN nucleation and growth. The higher deposition rate in the dual frequency mode can be correlated to the higher density of the plasma. The increase of the deposition rate indicates that precursor fragmentation and surface



decomposition are more efficient [3,4]. Thanks to "quasi insitu" XPS analysis with vacuum transfer (IMPACT/ADIXEN concept) which prevents samples from air-break oxidation, we are able to separate contributions in Ti2p region. In

particular, LF addition promotes TiC bonds (Fig.3 right) at a lower plasma power than standardly required in RF mode, which could result in lower damages on sublayers.

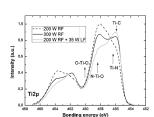


Figure 3: Left, growth rate of TiN deposited in RF mode only or in LF/RF mode, right, XPS Ti2p spectra of the corresponding films.

These plasma skills coupled with precursor engineering and characterization capabilities are in progress on advanced metal and alloys materials required for emerging applications in nanoelectronic.

Related Publications:

[1] R. Gassilloud et al., "A study of nitrogen behavior in the formation of Ta/TaN and Ti/TaN alloyed metal electrodes on SiO2 and HfO2

dielectrics", Appl. Phys. Lett., Vol. 104, 143501 (2014).
[2] F. Piallat et al., "Interface and plasma damage analysis of PEALD TaCN deposited on HfO2 by Angle Resolved XPS and C-V for advanced CMOS", App. Surf. Sci., 303, 388 (2014).
[3] F. Piallat *et al.*, "PECVD, RF vs Dual Frequency: investigation of plasma influence on metalorganic precursors decomposition and

material characteristics", J. Phys. D: Appl. Phys. 47, 185201 (2014).

[4] F. Piallat, "Plasma Assisted chemical deposition (CVD/ALD) and integration of Ti(Al)N and Ta(Al)N for sub-20nm metal gate", PhD Thesis, Univ. Grenoble Alpes, 2014.



#### Porous Silicon Based Maldi Platform for Medical Diagnosis

#### Research topics: Porous Silicon, Mass Spectrometry, Biomarker, Proteomic, Pathology

V. Aiello, A. Bouamrani, A. Mombrun, C. Leclech, F. Berger, F. Gaillard

Partnership: Clinatec Sponsorship: Carnot Funding

Few years ago, CEA-Leti has acquired a 200mm equipment dedicated to the (photo)-electrochemical anodisation of silicon in fluorhydric acid media (Fig.1). Such process allows the formation of porous silicon material owning nano, meso or macroporous characteristics. Not only because of its morphological aspect but also due to its mechanical, electrical and/or optical properties, porous silicon layer has generated many interests in the field of micro and nano (microsystem, biotechnology...). technologies energy, Recently, we have demonstrated a unique example of its interest for medical application and more particularly for the molecular analysis of biological fluids for early detection, prognosis and therapeutic response prediction of pathologies which represents a clinical challenge.

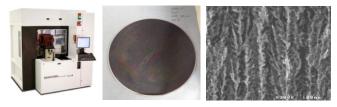


Figure 1: 200mm equipment for porous silicon fabrication.

Human serum is the body liquid that contains a richness of information concerning the overall pathophysiology of the organism. 99% of serum is composed of ubiquitous High Molecular Weight species (HMW), while the remaining 1% contains the Low Molecular Weight ones (LMW) potentially involved in the diagnosis of pathologies: the biomarkers. Their specific detection allows correlating a disease with the changes in the circulating proteins to improve diagnosis and to follow treatment efficacy and design personalized therapies with low invasiveness. Nowadays, Spectrometry (MS) and more particularly, MALDI-ToF (Matrix-Assisted Laser Desorption/Ionization -Flight), is considered a promising tool in terms of accuracy, response-time and costs and is currently used for molecular profiling. Nevertheless, the detection of LMW species needs prior preparing samples to reduce the large background of very abundant and non-relevant proteins. Traditional methods involve large sample volumes and time consuming protocols, but also potential pre-analytical bias due to sample handling and stability. Consequently, innovative technologies solving these issues are mandatory to easily

detect new biomarker. The development of nanomaterials, with controllable features at the nanometer level offered advantageous new physical properties and fostered the use of nanotechnology in biomedical applications.

We have demonstrated that mesoporous silicon layer, used as a platform for direct MALDI-ToF detection represents an efficient strategy for molecular size-exclusion (Fig.2). It allows fast and sensitive acquisition of proteomic profiles (less than an hour), and the detection of potential biomarkers in small volume of biological samples (few microliters). We have studied the influence of porous material characteristics (morphology, thickness...) on the enrichment of LMW species [1]. Thus, the most efficient porous layers with ordered, size-controlled structures and well-adjusted thicknesses have been identified and validated to individualize specific proteomic or metabolomic profiles of different pathological states (cardiovascular, lymphoma...).

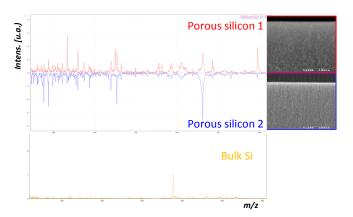


Figure 2: Enrichment of MALDI-ToF spectrum in the peptides range (2200-4000 m/z) on different porous silicon substrates (red, blue) compared to no-porous surface (orange).

In addition, a protocol has been developed to obtain low dimension 5x5mm squared samples from a 200mm etched silicon wafer [2]. It offers the ability to produce this porous silicon platform at a large scale which, for instance, will favor the biological analysis automation for epidemiologist study.

Related Publications:

[1] V. Aiello, A. Mombrun, C. Leclech, A. Bouamrani, F. Gaillard, "Study Of Porous Silicon Morphology Effects On Biomarker Detection", *E-MRS 2014 Spring Meeting*, May 27-29, 2014, Lille, France.

[2] V. Aiello, A. Mombrun, C. Leclech, A. Bouamrani, F. Gaillard, "Porous Silicon Based Maldi Platform for Diagnosis", 5<sup>th</sup> International BionanoMed 2014 Congress, March 26-28, 2014, Krems, Austria.



#### Ionic Liquids (ILs): an Innovative Medium for Nanofabrication

#### **Research topics: Nanoparticles, Nanofabrication**

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Partnership: CNRS-LC2P2, CNRS-SIMaP Sponsorship: Plateforme Nanochimie, ARC6 T.I.C.

Metallic nanoparticles (NPs) are needed in a range of such as the fabrication of advanced applications microelectronic, magnetic or optical devices. However, the controlled synthesis of metallic NPs in the range of 1 to 10 nm is still an on-going challenge, as is the understanding of their stabilization and agglomeration. In particular, substantial effort has been centered on stabilizing transitionmetal nanoparticles in wet synthesis processes. Unlike traditional solvents, ionic liquids (ILs) can be used to generate metallic NPs in the absence of any additive. Ionic liquids are molten salts at room temperature, composed of an organic cation and an inorganic or organic anion. They are thermally and electrochemically stable, non-volatile and electrically conductive. ILs can dissolve organometallic (OM) precursors, which have been shown to form metallic NPs by decomposition (or reduction) under dihydrogen. This process provides suspensions of metallic NPs, with accurate size control and high stability [1]. Hence, Ru, Cu, Ni, Mn and TaNPs have been synthesized under mild conditions.

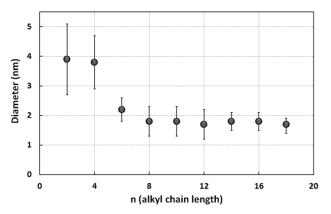


Figure 1: Size evolution of RuNPs with alkyl chain length (under 0.9 MPa H2 at 100°C for 4 h).

However, the exact mechanisms responsible for this stabilization remain unclear. Previous studies have shown that the size of RuNPs formed at 0°C could be related to a specific short-length order within the ILs, in which apolar alkyl ends of the cation organize into discrete, isolated pockets in a polar matrix. It turns out that the size of the RuNPs is comparable to and increases with the size of these apolar domains: the longer the alkyl chain, the larger the

NPs. Recently, attempts were made to synthesize RuNPs at 100°C and extended to ILs with longer chains [2]. In this case, the size decreases with chain length (Fig.1), probably driven by mass transport kinetics during the decomposition reaction.

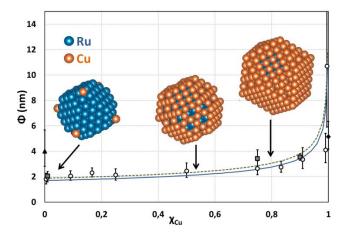


Figure 2: Diameter evolution of the RuCuNPs with Cu content as measured by TEM (white circles) and ASAXS (grey squares), and comparison with a model (layered icosahedral NPs with a 4-layer core and an increasing number of shell layers - for consistency, NPs composed of Cu only (solid line) or Ru only (dashed line) have been considered). Mono- and bimetallic NPs were formed by decomposition of the OM precursors in C1C4ImNTf2 for 4 h under 0.9 MPa H2.

Another interesting feature of this approach is the possibility to mix precursors to generate bimetallic NPs [3,4]. Suspensions of bimetallic nanoparticles (NPs) of Ru and Cu have been synthesized by simultaneous decomposition of two organometallic compounds in an ionic liquid. These suspensions have been characterized by Anomalous Small-Angle X-ray Scattering (ASAXS) at energies slightly below Ru K-edge. It is found that the NPs adopt a Ru-core, Cu-shell structure, with constant Ru core diameter of 1.9nm for all Ru:Cu compositions, while the Cu shell thickness increases with Cu content up to 0.9nm (Fig.2 [5]). The formation of RuCuNPs thus proceeds through rapid decomposition of the Ru precursor into RuNPs of constant size followed by the reaction of the Cu precursor and agglomeration as a Cu Thus, the different decomposition kinetics of precursors make possible the elaboration of core-shell NPs composed of two metals without chemical affinity.

#### Related Publications:

<sup>[1]</sup> Paul Campbell et al., "Ruthenium Nanoparticles in Ionic Liquids - A Saga", Current Organic Chemistry, 17(4), pp. 414-429, 2013.

<sup>[2]</sup> W Darwich et al., "Stabilization of mono- and bimetallic nanoparticles in ionic liquids", Nanotech2014, Vol.1, 2014.
[3] I.S. Helgadottir et al., "Synthesis of bimetallic nanoparticles in ionic liquids: Chemical routes vs physical vapor deposition", Microelectronic Engineering, 107(0), pp. 229-232, 2013.

<sup>[4]</sup> P. P Arquilliere et al., "Bimetallic Ru-Cu Nanoparticles Synthesized in Ionic Liquids: Kinetically Controlled Size and Structure", Topics in Catalysis, 56:1192-1198, 2013.

<sup>[5]</sup> I Helgadottir et al., "Ru-core/Cu-shell bimetallic nanoparticles with controlled size formed in one-pot synthesis", Nanoscale, 6(24):14856-14862, 2014.



#### **Direct Bonding Mechanism**

#### **Research topics: Advanced Substrate**

F. Fournel, C. Martin-Cocher, D. Radisson, V. Larrey, E. Beche, C. Morales, P.A. Delean, F. Rieutord, H. Moriceau, L. Di Cioccio, F. Baudin, P. Gergaud, V. Delaye, PJ. Jouneau, T. Signamarcheix, B. Imbert, X. Blot, T. Salvetat, E. Lagoutte, C. Lecouvey, T. Chaira, C. Bridoux, A.M. Papon, V. Carron, P. Gondcharton, L. Benaissa, M. Verdier, F. Madeira, G. Audoit, J.-M. Fabbri

#### Partnership: SOITEC, STMicroelectronics, CNRS Sponsorship: PIA-EXACT, Nano2017

Direct bonding is now a well-known technique to join two flat surfaces without any additional material. This technique is used in many applications and especially in SOI (Silicon-Onelaboration or in some backside imager manufacturing processes which are now almost in mass production. Oxide or metal direct bondings are then paying more and more a key role in microelectronic development. Direct bonding mechanism study is then very important in order to clearly understand this bonding behavior.

In the case of silicon and silicon oxide hydrophilic bonding  $(Si/SiO_2 \text{ or } SiO_2/SiO_2 \text{ bonding})$  we've shown that the bonding energy (adherence) evolution during the annealing was not due to the transition between van der Waals forces to covalent bonds [1]. Indeed, the gap shown on Fig.1a between the adhesion and the adherence energy at room temperature clearly indicates a covalent bonding presence even just after the bonding.

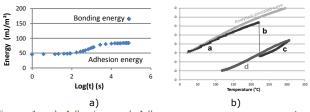


Figure 1: a) Adhesion and Adherence energy measurement of a chemical silicon direct bonding at room temperature. b) In situ bow an InP/GaAs annealing measurement during thermal for heterostructure pointing out a debonding/rebonding phenomenon

We've shown also that during post bonding annealing, the adherence energy evolution is more due to silicon oxidation between RT and 200°C for Si/SiO<sub>2</sub> bonding and to internal water stress corrosion for SiO<sub>2</sub>/SiO<sub>2</sub> bonding between RT and 500°C. Knowing this mechanism, the interface trapped water management allows us to optimize this bonding type.

In the same way, the study of the direct bonding mechanism of deposited alumina [2] leads to point out the crucial role of the trapped water. It enabled to greatly increase the interface quality of ALD-AL2O3 bonding has been as shown on Fig.2.

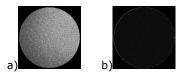


Figure 2: AL<sub>2</sub>O<sub>3</sub> bonding with a) amorphous or b) crystalized film.

Noteworthy, in this bonding type, instead of the bonding

interface, the deposited interface between the silicon and the alumina was mostly impacted by the bonding evolution.

Moreover from a mechanical point of view,, besides a generation of bonding defects, uncontrolled direct bonding interface evolution lead can to debonding/rebonding during the post bonding thermal treatment as shown for InP/GaAs heterostructure bonding [3], (cf. Fig.1b [b step]).

The direct bonding mechanism may even be more complex regarding other materials. For instance using ductile material as in metal direct bonding, we've shown that the bonding mechanism has to consider, for instance, the plasticity, the diffusion at grain boundaries and the specific atomic mobility in addition to the water management and the oxide formation/evolution [4].

For instance, in the case of copper/copper bonding, the specific characteristics of the copper oxide allow the bonding interface to be atomically closed even at room temperature inducing an interesting bonding energy increase as shown on

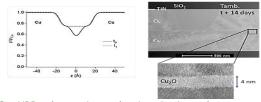


Figure 3: XRR observations showing in-time the copper oxide evolution at room temperature (left). It leads to a complete interface closure as shown in the TEM cross sections (right).

Specific copper properties may induce also during the annealing the oxide migration allowing a direct Cu-Cu contact. One can also note that the copper ability to deform plastically, to generate vacancies and to allow migration of these vacancies at the triple grain boundaries may lead to voids at the bonding interface (cf. Fig.4) whose formation mechanism has been studied in depth [5].

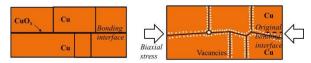


Figure 4: Voiding creation using vacancy accumulation mechanism during post-bonding annealing.

The same studies on titanium or tungsten direct bonding exhibit also very interesting mechanisms involving specific properties of each material [4].

#### Related Publications:

[1] F. Fournel, C. Martin-Cocher, D. Radisson, V. Larrey, E. Beche, C. Morales, P.A. Delean, F. Rieutord, H. Moriceau, "Water Stress Corrosion in Bonded Structures", ECS Transaction, 64(5) 121-132 (2014).

[2] E. Beche, F. Fournel, V. Larrey, F. Rieutord, C. Morales, A.-M Charvet, F. Madeira, G. Audoit, J.-M. Fabbri, "Direct Bonding Mechanism of ALD-Al<sub>2</sub>O<sub>3</sub> Thin Films", ECS Transaction, 64(5) 57-65 (2014).

[3] B. Imbert et al., "Mechanical understanding of 100mm InP and GaAs direct bonded heterostructure" Waferbond'13 (2013).

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[5] P. Gondcharton, B. Imbert, L. Benaissa, M. Verdier, "Voiding Phenomena in Copper-Copper Bonded Structures: Role of Creep", ECS

Transaction, 64(5) 357-367 (2014).





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